AD-A182 360 VLSI/VHSIC (VERY LARGE SCALE INTEGRATED/VERY HIGH SPEED INTEGRATED CIRCUI..(U) RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV K E CLARK DEC 86 RADC-TR-86-94 1/3

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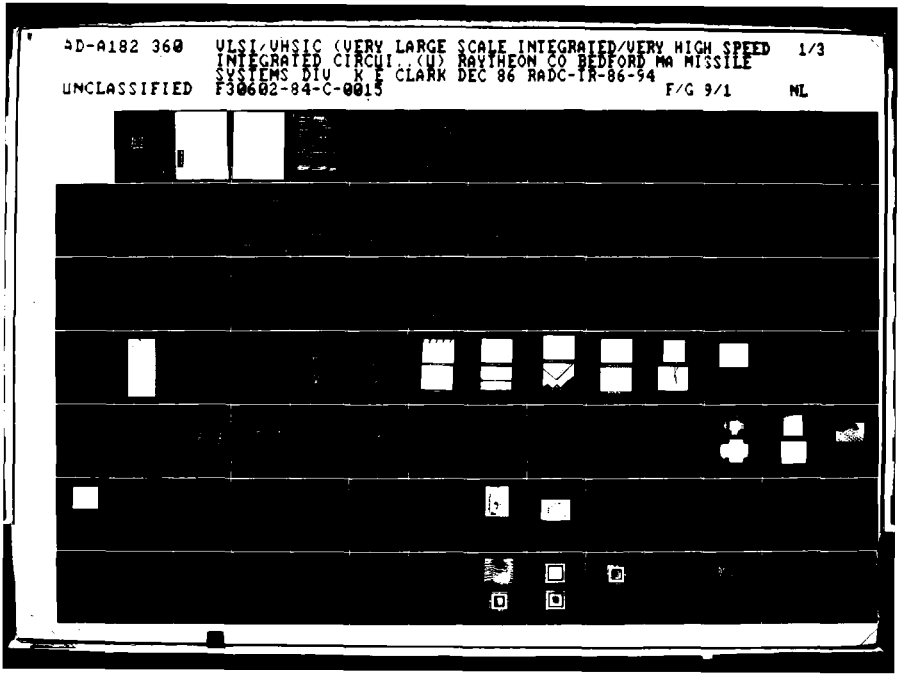

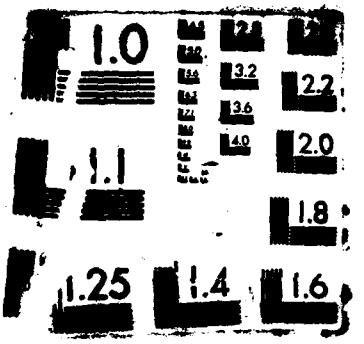
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AD-A182 340

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Very Large Scale Integrated and Very High Speed Integrated Circuits (VLSI/VHSIC), High I/O Count Packages, Microcircuit Packages (Cont'd)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The test methods of MIL-STD-883 were reviewed to assess their appropriateness in view of the new package styles and materials being used for VLSI/VHSIC devices. Experiments were performed to judge the effectiveness of existing tests. Changes to existing tests are proposed where deemed necessary and new tests are developed where no existing method adequately assesses new technology devices. Proposed changes and/or new package tests evaluate: solderability of leads; pin grid lead pull strength; leadless chip carrier bond strength; die attach bond analysis; characteristic impedance, capacitance, and delay time of high speed signals; crosstalk; and flip-chip pull strength.

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Block 18 (Cont'd)

Die Attach
High Speed Signals
Flip Chip
Hermeticity
Moisture Control
Military Standards (MIL-M-383510)
Military Test Methods (MIL-STD-883)

EVALUATION

The objective of this effort was to develop end-of-line or in-process test methods that will assure the quality and reliability of Very Large Scale Integration/Very High Speed Integrated Circuit (VLSI/VHSIC) packages. The result of this effort is a group of amended or new test methods that enhance the quality and reliability of packaged integrated circuits intended for qualification to military specifications.

The contractor has developed a change to the solderability test methods and has proposed seven entirely new package related tests. The seven tests are: 1) Pin Grid Array Lead Pull Test; 2) Ceramic Leadless Chip Carrier Bond Strength; 3) Ultrasonic Inspection of Die Attachment; 4) Microelectronics Package Digital Signal Transmission Assessment (characteristic impedance, capacitance, and delay time measurement procedures); 5) Crosstalk Measurement for Digital Microelectronics; 6) Ground and Power Supply Impedance Measurements; 7) Flip-Chip Pull-Off test.

The development of standard procedures, equipment, and test criteria for these package evaluations will prove to be a significant service to the VLSI/VHSIC device user community. In particular, the package electrical tests will allow users to select a package with the proper transmission characteristics to efficiently utilize the performance potential of high speed devices while meeting the compatibility requirements of the system in which the devices will be deployed.

The test methods developed in this effort will be reviewed by the military electronics community with the intention of submitting them for coordination to be included in MIL-STD-883. In addition to the tests developed, there are several clear areas the contractor reviewed that were beyond the scope of this effort which are worthy of further investigation. These tasks involve assessing the physical impact on packages and devices of certain testing technologies. These areas will be pursued in future investigations.

Eugene C. Blackburn

EUGENE C. BLACKBURN
Project Engineer

PREFACE

This study was conducted under Contract F30602-84-C-0015 by Raytheon Missile Systems Division, Bedford Laboratories, Product Assurance Group. The contract was administered under the technical direction of Mr. Eugene C. Blackburn of the Rome Air Development Center, Griffiss Air Force Base NY.

The results of a two-year survey of package test methods are reported here. The approach, test methods, samples, and evaluation plans were as stated in the proposal, "VLSI/VHSIC Package Test Development", with some mutually agreed upon modifications. More than twenty test methods or possible test methods were investigated. Seven new test methods were recommended for inclusion in MIL-STD-883. Modifications to two MIL-STD-883 methods were recommended.

Project Engineer was Ms. Kay Clark. Engineers contributing were Linda Cyr, James Hayes, David Pinsky, Timothy Reid, and Gerald Shulda. The management of Bedford Labs, Mr. Anthony Sansone, Manager Product Assurance, and Mr. Dieter Bartels, Supervisor, Product Assurance Laboratory, were instrumental in directing the efficient and timely administration of this effort.

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INTRODUCTION

As microcircuits increase in size and complexity to meet VHSIC program goals, demands on their packaging also increase. Packages for VLSI/VHSIC applications utilize configurations such as chip carriers, pin grid arrays and pad grid arrays rather than the standard dual-in-line (DIP) design. These new packages are larger, with more I/O terminations, and larger die cavities. Electrical interconnections from chip to package are made with configurations other than aluminum wires. At VHSIC frequencies (ultimate goals up to 100 MHz), the electrical properties of the package itself may become important.

These new packaging technologies will require new or enhanced MIL-STD-883 test methods. The purpose of this study was to evaluate the impact on MIL-STD-883 methods of five specific package design concerns:

- High I/O termination count
- Large area die
- High speed signal performance
- New geometries and methods of chip interconnection
- Large volume cavities.

The effectiveness of present methods was evaluated; modifications to conditions and limits were recommended; and new methods were developed where necessary.

The general approach to the study was experimental. Packages were tested to current methods when possible. Problem areas were then noted and changes recommended.

Some areas required new tests entirely. In these cases, a method was developed to the point of producing repeatable results. The method was then evaluated for effectiveness by subjecting parts to environmental stress tests and comparing environmental results to the test method results. This procedure was also used to set limits.

The data generated in the study was analyzed using standard statistical techniques. Some finite element analysis was also performed to aid in setting the limits of new test methods.

The following report gives details on the experimental results in each

of the five areas of concern. The report is structured in tasks as outlined below:

Definition of the Problem

Task 1: Survey of Package and Chip Vendors

Task 2: Finite Element Modelling

High I/O Termination Count

Task 3: Fixturing and Performance Criteria

Task 4: Specific Termination Characteristics

Large Area Die

Task 5: Die Attach Evaluation

High Speed Signal Performance

Task 6: Transmission Performance

Task 7: Crosstalk

Task 8: Ground Impedance

Task 9: Static (DC) Performance

Chip-to-Package Interconnection

Task 10: Bond Pull Effectiveness Evaluation

Task 11: Peel Test Evaluation

Task 12: Flip-Chip Evaluation

Large Volume Cavities

Task 13: Hermeticity and Moisture Control Evaluation

Each task report states the objectives, method, results, conclusions and summary for that portion of the study. Supporting reports, forms, data sheets and figures for each task are also included in that discussion. The proposed test methods and modifications, written in MIL-STD-883 format, are included as an Appendix to the report.

TASK 1: SURVEY OF PACKAGE AND CHIP VENDORS

OBJECTIVE

To determine industry trends in packaging and package test needs by surveying package vendors, chip vendors, and major users of microelectronic devices.

METHOD

A survey questionnaire concerning packaging techniques for VLSI/VHSIC microelectronic devices was prepared and distributed to both manufacturers and users. More than seventy surveys were sent out in direct mailing and approximately 100 additional copies were circulated at reliability and packaging conferences. A copy of the survey form follows this discussion on pages 5 through 17.

RESULTS

Fourteen surveys were returned from the respondents listed in Table 1.1. The results of the survey are tabulated on the copy of the form, pages 5 to 17. An asterisk (*) indicates the most frequent response. Longer responses which contain written explanations by the respondent are given in subsequent tables as noted. A discussion of the results follows these tables.

TABLE 1.1 - LIST OF RESPONDENTS TO SURVEY

Company, Location	Number of VLSI/VHSIC Devices Used/ Fabricated Per Year	
	No. Used	No. Fabricated
1. AMP, Inc. Harrisburg, PA	--	--
2. AT&T Bell Labs Allentown, PA	--	--
3. Control Data Corp. Minneapolis, MN	500 (15,000 by 1987)	
4. G.E. Pittsfield, MA	--	--
5. GTE Government Systems Needham, MA	37,000	37,000
6. Hazeltine Corp. Greenlawn, NY	250	--
7. Honeywell Underseas Systems Hopkins, MN	--	--
8. LSI Logic Corp. Milpitas, CA	--	3.6 Million
9. Magnavox Fort Wayne, IN	2 Million	--
10. Raytheon Sub. Sig. Div. Portsmouth, RI	10,000	--
11. Signetics, Corp. Sunnyvale, CA	--	20 Million
12. Sperry Corp. St. Paul, MN	> 1,000	> 1,000
13. TRW-CSI Products LaJolla, CA	--	Proprietary
14. Western Digital Corp. Newport Beach, CA	--	30 Million

SURVEY QUESTIONNAIRE

PACKAGING TECHNIQUES

OF

VLSI AND VHSIC MICROELECTRONICS

Prepared Under

Contract No. F30602-84-C-0015

For

United States Air Force
Air Force Systems Command
Rome Air Development Center
Griffiss Air Force Base, NY

Please answer all questions as completely as possible. For questions on time or quantity and selection of multiple choice, please use your best judgement.

Please return to: Raytheon Company, Missile Systems Division
Hartwell Road, Bedford, MA 01730

Attn: Kay Clark
Tel: (617) 274-7100 X4307
Keith Venuti
Tel: (617) 274-7100 X3665

DO YOU WISH TO HAVE THE RESULTS OF THIS SURVEY?

Question # 1

12* YES 2 NO

NAME OF COMPANY See Table 1.1

2 DIVISION/DEPARTMENT _____

ADDRESS _____

NAME OF RESPONDENT _____

POSITION _____

TEL. NO. _____

TYPE OF COMPANY BUSINESS _____

PRODUCTS INVOLVING VLSI/VHSIC TECHNOLOGY _____

3 Approximate Number of VLSI/VHSIC Devices:

Used Per Year See Table 1.1 Fabricated Per Year _____

The following questions are phrased in general terms. If more than one answer to a question is possible, please give that which most accurately reflects your VLSI/VHSIC activities.

4 Please check each activity performed by your Company/Division:

1 Manufacture VLSI/VHSIC packages.

6 Manufacture VLSI/VHSIC semiconductors.

7 Package chips in VLSI/VHSIC packages.

9* Assemble packaged devices into larger electronic systems.

9* Perform electrical tests on devices in VLSI/VHSIC packages.

6 Test devices in VLSI/VHSIC packages to MIL-STD 883.

5 Which of the following package styles do you currently use/produce/test? Please indicate the largest number of I/O's per each style presently in use and planned to be in use in 1984. (Typically 64 I/O or greater)

	Used Now	I/O's	Expected in 1985	I/O's
Leadless Chip Carriers	11	160	9	250
Leaded Chip Carriers	8	180*	8	180
Flat Packs	5	120	3	120
Pin-Grid Array	6	180*	6	224
Pad-Grid Array	5	88	2	250
Metal Hybrid Packages	5	88	5	140
Dual-In-Line	9	64	7	64
Other (Please specify)				
Plastic Chip Carrier	1	84	1	124
SOIC			1	20
Quad Plastic Cavity			1	312*

6 Please indicate the type(s) of lid sealing processes used or expected to be used in next 24 months. (If more than one type is involved, please check that which is most widely used.)

Metal/Metal	Now Used	Planned 24 Months
Seam Welding	3	4
One-Shot Welding	3	2
Eutectic (e.g., Au/Sn)	9*	7*
Solder (e.g., Pb/Sn)	4	3
Other (Please specify)		
Epoxy	1	1
Low cost Pb/Sn	0	1
Sealing Glass	4	4
Polymer	4	4
Other (Please specify)		
_____	_____	_____

7 Do you/will you use a polymeric coating material on the chips prior to sealing?

3 Yes 10* No

	Now Used	Planned 24 Months
Parylene	_____	3*
Silicone	2*	1
Other (Please specify)	_____	_____
_____	_____	_____

8 Please complete the Table for each package style produced/used/tested:

a Style:
- Leadless Chip Carrier 12*
- Leaded Chip Carrier 8
- Flat Pack 3
- Pin-Grid Array 6
- Pad-Grid Array ___
- Metal Hybrid Cans 5
- Dual-In-Line 7

b Manufacturer: See Table 1.2

c No. of I/O's (circle)

≤64	≤100	≤150	≤200
(18*)	(10)	(8)	(3)

d Terminal Spacing (in) (circle)

.025	.050	.100
(7)	(21*)	(14)

e Cavity Volume (cc) (circle)

≤0.40	>0.40
(19*)	(17)

f Largest Dimension (in) (circle)

≤.5	≤1.0	≤2.0	≤3.0	>3.0
(2)	(8)	(20*)	(5)	(2)

g No. of Layers (circle)

1	2	3	4	>4
(4)	(2)	(17*)	(5)	(2)

h Die Attach: epoxy-non-conductive 3; polyimide 4; solder perform 15; conductive 20*; silver glass 5

Please complete the Table for each package style produced/used/tested:

Style:
- Leadless Chip Carrier ___
- Leaded Chip Carrier ___
- Flat Pack ___
- Pin-Grid Array ___
- Pad-Grid Array ___
- Metal Hybrid Cans ___
- Dual-In-Line ___

Manufacturer: _____

No. of I/O's (circle): ≤64 ≤100 ≤150 ≤200

Terminal Spacing (in) (circle): .025 .050 .100

Cavity Volume (cc) (circle): ≤0.40 >0.40

Largest Dimension (in) (circle): ≤.5 ≤1.0 ≤2.0 ≤3.0 >3.0

No. of Layers (circle): 1 2 3 4 >4

Die Attach: epoxy-non-conductive ___; polyimide ___; solder perform ___; conductive ___; silver glass ___

THIS PAGE REPEATED FROM SURVEY FORM

Please complete the Table for each package style produced/used/tested:

Style: Leadless Chip Carrier ___
Leaded Chip Carrier ___
Flat Pack ___
Pin-Grid Array ___
Pad-Grid Array ___
Metal Hybrid Cans ___
Dual-In-Line ___

Manufacturer:_____

No. of I/O's (circle)	≤64	≤100	≤150	≤200	
Terminal Spacing (in) (circle)	.025	.050	.100		
Cavity Volume (cc) (circle)	≤0.40	>0.40			
Largest Dimension (in) (circle)	≤.5	≤1.0	≤2.0	≤3.0	>3.0
No. of Layers (circle)	1	2	3	4	>4

Die Attach epoxy-non-conductive ____ polyimide ____ solder perform ____
conductive ____ silver glass ____

Please complete the Table for each package style produced/used/tested:

Style: Leadless Chip Carrier ___
Leaded Chip Carrier ___
Flat Pack ___
Pin-Grid Array ___
Pad-Grid Array ___
Metal Hybrid Cans ___
Dual-In-Line ___

Manufacturer:_____

No. of I/O's (circle)	≤64	≤100	≤150	≤200	
Terminal Spacing (in) (circle)	.025	.050	.100		
Cavity Volume (cc) (circle)	≤0.40	>0.40			
Largest Dimension (in) (circle)	≤.5	≤1.0	≤2.0	≤3.0	>3.0
No. of Layers (circle)	1	2	3	4	>4

Die Attach epoxy-non-conductive ____ polyimide ____ solder perform ____
conductive ____ silver glass ____

INTERCONNECTIONS

Please answer all questions which apply to your packaging/assembly styles.

9 **Semiconductor Chips To Package:**

What method do you or will you use to electrically connect semiconductor chips to the package? Please check below the method now most widely used and expected to be used in 1985:

	Used Now	Expected in 1985
Wire Bonding	14*	11*
Tape Automated Bonding	3	3
Flip Chips		1
Beam Leads	1	1
Other (Please specify)		

10 **Wire Bonding**

If more than one method or material is used, please indicate dominant one:

a. Wire Material(s) See Text

b. Wire Size(s) See Text

c. Method of Bonding:

	Constant-Temp. Thermocompression	5	Thermosonic
	Pulsed-Capillary Thermocompression	9*	Ultrasonic
	Other (Please specify)		

7 Manual 10* Automated

11 Tape Automated Bonding

a Tape Format(s) Used: (Please check most widely used format.)

____ 8 mm ____ 11 mm ____ 12.5 mm _1_ 14 mm _1_ 16 mm

____ 17.5 mm ____ 19 mm _2*_ 35 mm Other (Please specify)_____

b Laminated Metal _3*_ Cu _____ Al

c Does the format(s) meet ASTM Document 7E45 requirements? _2*_ Yes _1_ No

d Tape used, current and/or planned, is:

_2*_ One-layer _1_ Two-layer ____ Three-layer _1*_ Testable

____ Non-Testable _1*_ Bumped (Bonding bump formed on Tape)

____ Unbumped

e _2_ Made In-House _2_ Purchased from Outside Vendor

(Please name: 3M, none others specified)

f Chips used, current and/or planned, are:

_1_ Bumped (Bonding bump formed on Chips) _5*_ Unbumped

____ Purchase from Outside Vendor _3*_ Make _2_

(Please name:_____)

12 **Inner Lead Bonding:**

3* Thermocompression (e.g., Gold-Gold) 0 Fusion (e.g., Gold-Tin)

Equipment Manufacturer: Jade; none others specified

13 **Outer Lead Bonding:**

3* Thermocompression 2 Solder

Equipment Manufacturer: Jade; none others specified

14 **Flip-Chips:**

Chips are procured from:

Outside Supplier 1 % In-House Fab. 1 %

Bonding is: (no responses)

____ Solder ____ Solder, Controlled Collapse ____ Ultrasonic

____ Other (Please specify)_____

15 **Beam-Leads:**

Chips are procured from:

Outside Supplier 1 % In-House Fab. 2* %

Bonding is:

1* Compliant ____ Wobble-Bonding

____ Other (Please specify)_____

TESTING

If you perform tests to MIL-STD-883, please answer the following questions. Refer to the following table for lists of relevant tests.

16 All the packages and devices you required to test meet the Class B requirements of MIL-STD-883?

	9* Yes	0 No
Class S?	1 Yes	6* No

17 Which tests do you consider excessive for your packaging/assembly styles? (Please list by method no. a reference Table has been included).

1. (see Table 1.3) 3._____ 5._____ 7._____

2._____ 4._____ 6._____ 8._____

For what reason(s) do you consider these tests excessive?

1. (see discussion)
2.
3.
4.
5.
6.
7.
8.

18 Which tests do you consider irrelevant to your packaging/assembly styles? (Please list by method no.) (see Table 1.4)

1._____ 3._____ 5._____ 7._____

2._____ 4._____ 6._____ 8._____

19 What other documents are used on military contracts?

MIL-M-28787 MIL-M-38510 MIL-Q-9858 _____

_____ _____ _____ _____

20 a Please indicate types of specifications used:

6 Company Approved Only 8* Customer Approved

3 Customer Baseline _____ Other (Please specify)_____

b Manufacturing Inspection:

_____ None 3 Sample 6* 100% 1 Surveillance

c Quality Assurance Inspection:

_____ None 8* Sample 1 100% 1 Surveillance

21 What do you consider the major limitation(s) to be in packaging of VLSI/VHSIC Microcircuits for Military Applications?

	Now	By 1985
Hermeticity	1	1
Mechanical Problems	7	6
Thermal Problems	6	8*
Testing	8*	8*
Interconnections	3	5

Other (Please specify) Now: Process control, material limitations,

By 1985: eutectic die attach on large chips.

Please add any other comments or suggestions on separate attached sheets.

What do you consider the major limitation(s) to be in packaging of VLSI/VHSIC Microcircuits for Military Applications?

	Now	By 1985
Hermeticity	_____	_____
Mechanical Problems	_____	_____
Thermal Problems	_____	_____
Testing	_____	_____
Interconnections	_____	_____

Other (Please specify) Now: _____

By 1985: _____

Please add any other comments or suggestions on separate attached sheets.

TEST METHODS

Method No.	Environmental Tests
1001	Barometric pressure, reduced (altitude operation)
1002	Immersion
1003	Insulation resistance
1004.4	Moisture resistance
1005.4	Steady state life
1006	Intermittent life
1007	Agree life
1008.2	Stabilization bake
1009.4	Salt atmosphere (corrosion)
1010.5	Temperature cycling
1011.4	Thermal shock
1012.1	Thermal characteristics
1013	Dew point
1014.5	Seal
1015.4	Burn-in test
1016	Life/reliability characterization tests
1017.2	Neutron irradiation
1018.2	Internal water-vapor content
1019.2	Steady state total dose irradiation procedures
1020	Radiation induced latchup test procedure
1021	Dose rate threshold for upset of digital microcircuits
1022	Mosfet threshold voltage
1023	Dose rate response of linear microcircuits
1030	Preseal burn-in
1031	Thin film corrosion test

	Mechanical Tests
2001.2	Constant acceleration
2002.3	Mechanical shock
2003.3	Solderability
2004.4	Lead integrity
2005.1	Vibration fatigue
2006.1	Vibration noise
2007.1	Vibration, variable frequency
2008.1	Visual and mechanical
2009.4	External visual
2010.7	Internal visual (monolithic)
2011.4	Bond strength
2012.5	Radiography
2013.1	Internal visual
2014	Internal visual and mechanical
2015.4	Resistance to solvents
2016	Physical dimensions
2017.3	Internal visual (hybrid)
2018.1	Scanning electron microscope (SEM inspection of metallization)
2019.2	Die shear strength

TEST METHODS

Method No.	Mechanical Tests (Continued)
2020.3	Particle impact noise detection test
2021.1	Glassivation layer integrity
2022	Meniscograph solderability
2023.1	Nondestructive bond pull
2024.2	Lid torque for glass-frit-sealed packages
2025.1	Adhesion of lead finish
2026	Random vibration
2027	Substrate attach strength
	Electrical Tests (digital)
3001.1	Drive source, dynamic
3002.2	Load conditions
3003.1	Delay measurements
3004.1	Transition time measurements
3005.1	Power supply current
3006.1	High level output voltage
3007.1	Low level output voltage
3008.1	Breakdown voltage, input or output
3009.1	Input current, low level
3010.1	Input current, high level
3011.1	Output short circuit current
3012.1	Terminal capacitance
3013.1	Noise margin measurements for digital microelectronic devices
3014	Functional testing
3015.2	Electrostatic discharge sensitivity classification
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4001	Input offset voltage and current and bias current
4002	Phase margin and slew rate measurements
4003	Common mode input voltage range Common mode rejection ratio Supply voltage rejection ratio
4004	Open loop performance
4005	Output performance
4006	Power gain and noise figure
4007	Automatic gain control range
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5001	Parameter mean value control
5002	Parameter distribution control
5003	Failure analysis procedures for microcircuits
5004.6	Screening procedures
5005.8	Qualification and quality conformance procedures
5006	Limit testing
5007.5	Wafer lot acceptance
5008.2	Test procedures for hybrid and multichip microcircuits
5009.1	Destructive physical analysis
5010	Test procedures for custom monolithic microcircuits

The results of the survey are discussed in detail below. Responses are summarized by question number, referring to the questions on the survey form.

Question

1 — Of the 14 respondents, 12 wished to have the results of the survey, while 2 did not.

2, 3 — See Table 1.1.

4 — The most common VLSI/VHSIC activities performed by the respondents are assembling packaged devices into larger electronic systems and performing electrical tests on devices in VLSI/VHSIC packages. A slightly smaller number manufacture VLSI/VHSIC semiconductors, package chips in VLSI/VHSIC packages, or test devices in VLSI/VHSIC packages to MIL-STD-883. The majority of the respondents were engaged in more than one activity. Only one respondent manufactures VLSI/VHSIC packages.

5 — Of the package styles listed, all but pad-grid array packages show widespread use, with leadless chip carriers being the most popularly used package style. Dual-in-line packages and leaded chip carriers were nearly as popular. Two respondents plan to begin using or fabricating pad-grid array packages by 1985. The I/O's column contains the largest number of I/O pins mentioned for each package style. The largest number of I/O's in use now is 180, in leaded chip carriers and pin-grid array styles. In 1985, a quad plastic cavity package is expected to have 312 I/O's, while the number of I/O's is also expected to increase for most other package styles.

6 — The most common lid sealing process indicated by the respondents is eutectic (gold-tin) seal, for both now and the next 24 months. The remaining responses were divided fairly equally among seam welding, one-shot welding, solder, sealing glass, and polymer sealing methods. One respondent uses epoxy, and one plans to use a low-cost Pb/Sn method within 24 months.

7 — Only 3 respondents now use or plan to use a polymeric coating on the chips prior to sealing. All three of these plan to begin using parylene within 24 months; two now use silicone and the other plans to begin using silicone within 24 months.

Question

8 Question 8 is a table containing the characteristics of each package style the respondents currently produce, use or test. Compiled, the tables indicate which package characteristics are currently the most common.

a) These numbers essentially reflect the responses to Question 5.

b) A list of manufacturers mentioned and the frequency of their mention is given in Table 1.2.

c) Nearly one-half of the packages mentioned contain 65 or fewer I/O's. Most of the rest have 150 or fewer I/O's, while only 3 packages have 150-200 I/O's.

d) One-half of the packages reported have a terminal spacing of 0.050 in. One-third have a spacing of 0.100 in., while the remaining one-sixth have a spacing of 0.025 in.

e) Just over one-half of the packages reported have a cavity volume under 0.40 cc. Just under one-half have a cavity volume over 0.40 cc.

f) The largest dimension on the reported packages is most commonly between 1.0 and 2.0 in. Only one package style mentioned had a dimension greater than 3 in.

g) More than one-half of the packages reported are constructed with three layers. Of the rest, most are constructed with one, two, or four layers. Only two packages are mentioned with more than 4 layers.

h) Of the die attach methods listed, the conductive epoxy and solder preform methods, respectively, are most frequently used. The non-conductive epoxy, polyimide, and silver-glass die attach methods together account for only one-quarter of the total number.

9 For electrically connecting semiconductor chips to packages, the wire bonding method is predominantly used. Tape automated bonding and beam leads are also mentioned but their use is not expected to grow in the next year. One respondent plans to use flip chips by 1985.

TABLE 1.2 - LIST OF MANUFACTURERS OF VLSI/VHSIC PACKAGES

REPORTED BY RESPONDENTS

Manufacturer	No. of Occurrences
Kyocera	17
3M/GE	8
NTK	3
Intel	2
Signetics	2
AMP	1
Bourns	1
Honeywell	1
Isotronics	1
Total	36

Question

10

a) The respondents mentioned two wire materials used in their wire bonding processes. Ten of the respondents use a wire composed of 99 percent aluminum, 1 percent silicon. Five respondents mentioned the use of gold wire.

b) The most common wire size reported is 1.25 mil (by 9 respondents). Seven respondents use a wire size of 1.00 mil. Other wire sizes receiving mention are 0.7 mil, 1.3 mil. 1.5 mil, and 2.0 mil.

c) Only ultrasonic (9 respondents) and thermosonic (5) bonding methods are used by the respondents. Ten respondents use automated bonding processes, while 7 use manual wire bonding (e.g., three respondents do both).

11

Only three respondents answered questions in the Tape Automated Bonding Section of the survey.

a) Two reported the use of 35 mm tape format, while 14 mm and 16 mm formats also received mention.

b) The laminated metal used by all three respondents is copper.

c) Two of the respondents reported that their formats meet ASTM document 7E45 requirements, one did not.

d) Two respondents use one-layer tape, one uses two-layer tape. One reported that the tape used is testable, and another reported that the tape used is bumped.

e) One respondent manufactured the tape, one reported that he purchased tape from 3M; the other respondent both manufactures and purchases tape, but did not mention the vendor.

f) The chips used in the tape automated bonding process are primarily unbumped (5) as opposed to bumped (1). Three respondents purchase chips from an outside vendor, while two manufacture their chips.

Question

12 In the process of inner lead bonding, only thermocompression (3) is in use by the respondents. Jade is the only equipment manufacturer specified.

13 In the process of outer lead bonding, 3 respondents use the thermocompression, while two respondents use solder. Jade again is the only equipment manufacturer specified.

14 One respondent reported the manufacture of flip-chips, another procured them from an outside supplier. No other responses were received in this section.

15 Two respondents fabricate chips for beam-leads: one respondent procures the chips from an outside supplier. One respondent reported that the bonding is compliant.

16 Of the nine respondents who test VLSI/VHSIC packages, all of them test to MIL-STD-883. Only one of those respondents, however, tests to Class S requirements.

17 Seventeen separate tests received mention by the respondents who answered (7) as being excessive for their packaging/assembly styles. They are listed in Table 1.3.

Test 2001 (Constant Acceleration) was mentioned by three respondents as being excessive. All three considered the 30,000 G test limit too high, placing excess stress on VLSI packages. One respondent recommended a test limit of 20,000 G.

Two respondents considered test 2010 (Internal visual, monolithic) not practical for VLSI chips since only top surface defects can be seen with high magnification. One respondent recommended an alternate screening procedure per paragraph 3.3 of test 5004.

Refer to Table 1.3 for a complete list of excessive tests as given by the respondents.

18 Only two respondents listed any tests as being irrelevant to their packaging/assembly styles - one respondent listed one test, while the other listed nine. A list of these tests is included as Table 1.4.

TABLE 1.3 - MIL-STD-883C TESTS CONSIDERED EXCESSIVE BY RESPONDENTS

Test No.	Test Name	Frequency of Mention
2001	Constant acceleration	3
2010	Internal visual (monolithic)	2
2020	Particle impact noise detection	2
1009	Salt atmosphere (corrosion)	2
1001	Barometric pressure, reduced (altitude operation)	1
1002	Immersion	1
1004	Moisture resistance	1
1008	Stabilization bake	1
1017	Neutron irradiation	1
1014	Seal	1
1019	Steady state total dose irradiation procedure	1
1020	Radiation induced latchup test procedure	1
1021	Dose rate threshold for upset of digital microcircuits	1
1023	Dose rate response of linear microcircuits	1
1030	Preseal burn-in	1
2003	Solderability	1
2027	Substrate attach strength	1

TABLE 1.4 - MIL-STD-883C TESTS CONSIDERED IRRELEVANT BY RESPONDENTS

Respondent	Test No.	Test Name
Sperry Corp.	1001	Barometric pressure. reduced (altitude operation)
Sperry Corp.	1002	Immersion
Sperry Corp.	1009	Salt atmosphere (corrosion)
Sperry Corp.	1020	Radiation induced latchup test procedure
Sperry Corp.	2002	Mechanical shock
Sperry Corp.	2005	Vibration fatigue
Sperry Corp.	2006	Vibration noise
Sperry Corp.	2007	Vibration, variable frequency
Sperry Corp.	2026	Random vibration
Magnavox	2001	Constant acceleration

Question

19 Three other documents are used by the respondents on military contracts. They are: MIL-M-28787, MIL-M-38510 and MIL-Q-9858.

20 a) The majority (8) of the respondents use customer-approved specifications. A slightly smaller number (6) use only company approved specifications. Three respondents use customer baseline specifications.

b) The method of manufacturing inspection most used by the respondents is 100 percent inspection (6). Three use sample inspection, and one uses surveillance inspection.

c) Eight respondents reported using sample quality assurance inspection. One reported 100 percent inspection, and one used surveillance inspection.

21 In the packaging of VLSI/VHSIC microcircuits for military applications; testing, mechanical problems, and thermal problems are the major concerns of the respondents both for 1984 and in 1985. Interconnections are expected to become a greater limitation by 1985, while hermeticity is considered to be a major limitation by only one respondent.

CONCLUSIONS

The survey showed that I/O count was expected to increase, chip carriers (leadless and leaded) would be the most commonly used configuration, epoxies would be used for die attach, and aluminum wire bonds were still the most common interconnection. A few companies were beginning to use tape bonding, and some used polyimide and silver-glass die attach. Most of the responses indicated that the majority would continue with established, available packaging technologies.

TASK 2: FINITE ELEMENT MODELLING

OBJECTIVE

Finite element modelling was used to extend test results to different package geometries where only a limited number of package sizes, etc. were available as samples.

DISCUSSION

Structural calculations for many mechanical systems can be accomplished using finite element modelling. The physical properties of the package (or any structure) are translated into an analytical model consisting of idealized "elements" connected at different grid points. Physical loads can be placed on some grid points with the subsequent effect calculated throughout the structure. The elements contain information on material properties, mass distribution, and other structural information required for the calculation. The grid points were set by the geometry of the package. A schematic representation of the technique is shown in Figure 2.1.

The actual calculations were performed using two computer programs: PATRAN-G and MSC/NASTRAN. PATRAN-G was used to define the geometric model. The program generates both a representation of the major regions describing the model and the finite element model used as input to NASTRAN. The program can display the model with color-coding due to stresses, deformation, etc. The MSC/NASTRAN program provided the analysis of the model. Loads could be applied at grid points to determine effects on the entire structure.

These analytical tools were intended for use in support of actual test results. The approach was to model a given test configuration, then predict behavior trends with changes to the geometry or applied stress.

Two models were generated during this study: the chip carrier push test, and the flip-chip pull test. For the chip carrier, the effect of increased package perimeter (and the subsequent increased number of solder joints) on the stress at the terminals due to a pushing force was investigated. The results were used to set limits for this test method. Similarly, the flip-chip model was used to determine the effects of stress on the solder bumps in response to a pulling force on the chip. These responses were used to set the limit on the flip-chip pull test method.

In both cases, results were discussed within the Task section of the test methods. These are Task 4 for the chip carrier push test, and Task 12 for the flip-chip pull test.

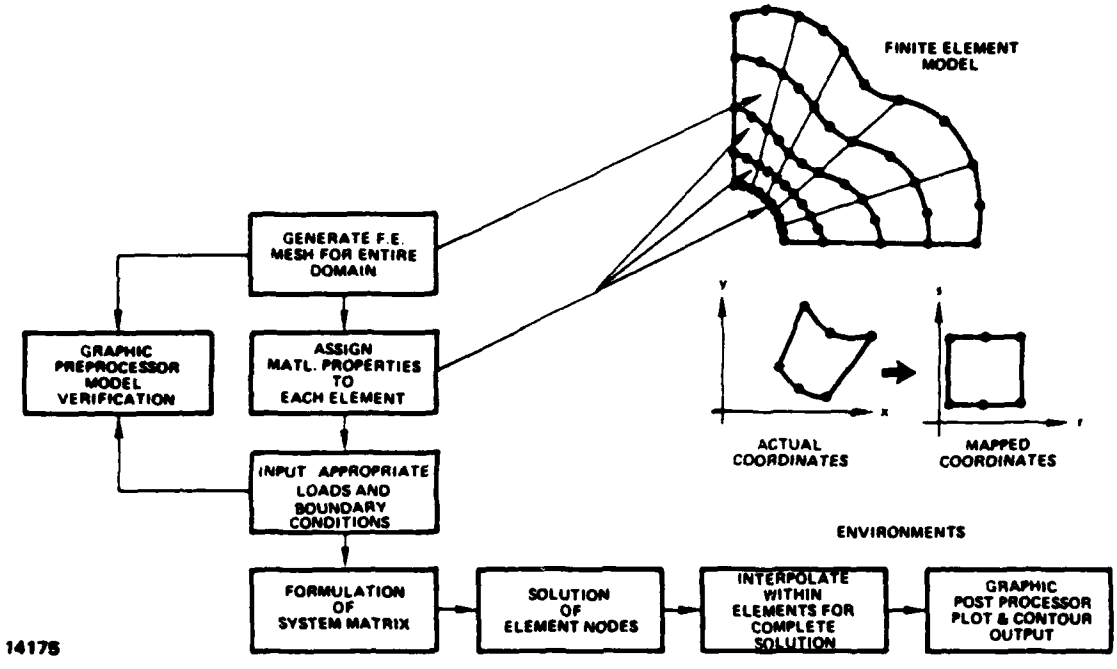


Figure 2.1 - FEM Flow Chart.

The finite element modelling approach proved helpful in predicting the behavior of stresses on chip carrier and flip-chip solder joints for geometries that were not available for testing. However, the main emphasis of the study was in the experimental results, with modelling serving as an aid to setting test limits.

TASK 3: FIXTURING AND PERFORMANCE CRITERIA

OBJECTIVE

To assess the impact of high lead count and large size packages on fixturing for MIL-STD-883 tests, and to determine which tests and performance criteria need to be modified to accommodate these packages.

METHOD

The four high lead count package types chosen for this task were 180 I/O pin grid array, 180 I/O pad grid array, 132/25 flat pack, and 132/25 leadless chip carrier. Five packages of each type were used during the test.

The following MIL-STD-883 tests were chosen as test methods that address large package size, greater fragility of the leads, and the larger seal area of the package: Temperature Cycling (Method 1010), Constant Acceleration (Method 2001), and Mechanical Shock (Method 2002). Hermeticity tests (Method 1014, Conditions A_1 and C) were used to indicate failures. Fixturing was necessary for adequate support of all packages during Constant Acceleration and Mechanical Shock tests. Two plexiglass fixtures were constructed: the grid array packages differed only in the pins (for which individual holes were drilled) and used the same fixture. The same was true for the two chip carrier styles; the package sizes were identical, and allowing space for the leads of the flat pack still maintained support of the leadless chip carrier. The two fixtures are shown in Figure 3.1.

The test procedure for all packages follows. All tests were performed at Class B levels.

1)	Initial Fine, Gross Leak	(both @ 60 $\pm$ 2 psig, 2 hours)
2)	Constant Acceleration	(30,000 G, Y1)
3)	Fine, Gross Leak	
4)	Mechanical Shock	(1500 G, 0.5 msec, Y1)
5)	Fine, Gross Leak	
6)	Temperature Cycle	(-65°C to +150°C, 10 cycles)
7)	Final Fine, Gross Leak	

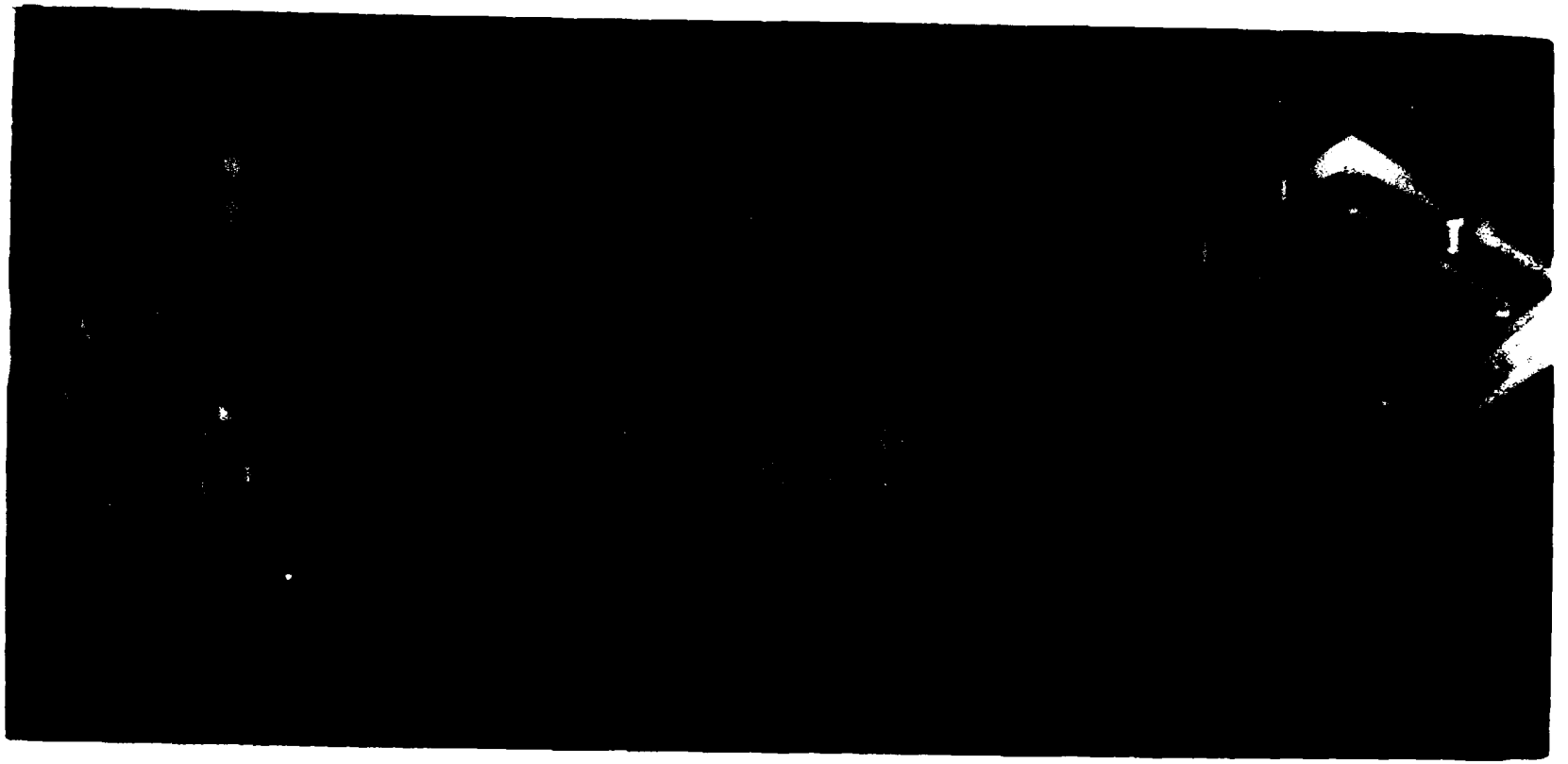


Figure 3.1 - Photograph of fixtures used to support packages during Constant Acceleration and Mechanical Shock testing.

RESULTS

When the 180 I/O pin-grid array packages were fine leak tested to Condition A_1 of Method 1014 following a 10-minute dwell-time, three of three parts were shown to fail (R_1 = 1.3 x 10^{-7}, 7.4 x 10^{-8} and 7.6 x 10^{-8} atm-cc/sec compared to reject limit 5 x 10^{-8} atm-cc/sec). After a 55-minute dwell time at ambient conditions, all 3 units passed (R_1 = 2.5 x 10^{-8}, 1.8 x 10^{-8}, and 1.8 x 10^{-8}). Apparently helium adsorbed on the package surface was giving a false leak reading.

A bake-out time was added after bombing to drive off the adsorbed helium and accelerate the necessary dwell time. It has been demonstrated that the effect of a post-bomb bake out on the Howl and Mann Equation used to set limits in Method 1014, Condition A_2, is to replace the dwell time, t_2, with an effective dwell time, t_2', as shown below:

$$t_2' = t_2 + t_B \left(\frac{T_B}{T_o}\right)^{1/2}$$

where t_2' = dwell time with bake-out

t_2 = dwell time

t_B = time duration of bake-out

T_B = temperature of bake-out in °K

T_o = ambient temperature in °K

Assumptions made in deriving this "effective" dwell time were consistent with those made to derive the Howl and Mann Equation. For a bake-out of 10 minutes at 100°C, this equation shows:

$$t_2' = 11.19 \text{ minutes} + t_2$$

Thus adding a bake-out would require a subsequent dwell time of less than 48 minutes to meet the 1-hour dwell time requirement for the fixed conditions of A_1. This approach was used to make all fine leak hermeticity measurements on the large packages.

The data sheets from the tests are shown in Figures 3.2 and 3.3. All of the packages passed initial fine and gross leak testing when performed as described above. After Constant Acceleration, one 132/25 flat pack failed fine and gross leak testing. Visual examination revealed a crack in the glass seal of the package. The crack is shown in Figure 3.4. A dye penetrant test was then performed to verify leakage at this site. Figure 3.5 shows the infused dye (Zyglo illuminated with ultra-violet light) emerging from the package at the crack.

Leak testing after Mechanical Shock revealed four failures: two leadless chip carriers and two pin-grid arrays. Figures 3.6 through 3.8 show the dye penetrant photographs and holes in the lid seals of the two failed leadless chip carriers and one of the pin grid arrays. When all the samples for this test sequence were first assembled, there were difficulties in producing a good lid seal. The lid seal procedure was repeated at least twice on some package styles, and was followed by touch-up soldering on others. Apparently the majority of the shock failures reflected this poor initial sealing rather than overstress induced by the test method.

The other pin grid array failure (see Figure 3.9) was due to both a poor lid seal and breaks in the package ceramic. The pattern of the cracks indicates that the package flexed in the direction of the acceleration. Failures of this type often occur when the ceramic and lid were not supported evenly in the test fixture. Adding a compressible material to the lid support area would prevent future fixturing problems.

All of the remaining packages passed through temperature cycling and final fine and gross leak testing without difficulty.

CONCLUSIONS

Hermeticity (fine and gross leak) tests are adequate and appropriate for these packages, provided the dwell time is sufficient to remove adsorbed helium. This can be accomplished by increasing the time at room temperature and using the flexible method of A_2; or by adding a short bake-out after bombing and applying the fixed method limits.

No difficulties were experienced in performing the Temperature Cycle test. The large size, high lead count packages do not present a need for modification of the accept/reject criteria for this test.

There were no difficulties in performing the Constant Acceleration test once adequate fixtures were built. Since the majority of the samples passed the highest possible test limit of 30,000 g's, there is no reason to reduce this limit. The failure of the one 132/25 flat pack does show, however, that some package styles may be more susceptible to breaking during test than others. Packages must be selected in design that can meet the required test condition for the application.

TEST DESCRIPTION:

LCC Eval.

Ser. No. #	INITIAL FINE LEAK	INITIAL GROSS LEAK	POST ACCELL. FINE LEAK	POST ACCELL. GROSS LEAK	POST MECH SHOCK FINE LEAK	POST MECH SHOCK GROSS LEAK	POST TEMP CYCLE FINE LEAK	POST TEMP CYCLE GROSS LEAK
Leads								
1	2.6×10^{-9}	Pass	4.2×10^{-9}	Pass	4.8×10^{-9}	Pass	5.2×10^{-9}	Pass
2	2.2×10^{-9}	Pass	2.0×10^{-8}	Fail	—	—	—	—
3	2.0×10^{-9}	Pass	3.2×10^{-9}	Pass	2.8×10^{-9}	Pass	3.6×10^{-9}	Pass
4	2.0×10^{-9}	Pass	2.8×10^{-9}	Pass	2.8×10^{-9}	Pass	3.6×10^{-9}	Pass
5	2.0×10^{-9}	Pass	3.6×10^{-9}	Pass	2.8×10^{-9}	Pass	3.6×10^{-9}	Pass
Pads								
6	1.8×10^{-9}	Pass	4.8×10^{-9}	Pass	2.4×10^{-9}		2.8×10^{-9}	Pass
7	1.8×10^{-9}	Pass	3.6×10^{-9}	Pass	Fail	Fail	—	—
8	1.6×10^{-9}	Pass	3.8×10^{-9}	Pass	Fail	Fail	—	—
9	1.6×10^{-9}	Pass	3.8×10^{-9}	Pass	2.9×10^{-9}	Pass	8.6×10^{-9}	Pass
10	1.6×10^{-9}	Pass	3.4×10^{-9}	Pass	2.4×10^{-9}	Pass	2.8×10^{-9}	Pass

TEST COMMENTS:

ACCELL., 30,000 Gs Y1 RJB 1-10-85

MECH. SHOCK, 1,500 Gs .5 MIL. SEC. Y1 RJB 1-10-85

TEMP. CYCLE, -65 +150 10 CYCLES RJB 1-15-85

VISUAL:

POST ACCELL. RJB 1-10-85

POST MECH. SHOCK RJB 1-11-85

POST TEMP. CYCLE RJB 1-15-85

INITIAL: ____

DATE: ____

TEMP.: ____

HUMIDITY: ____

CHECKED BY: ____

TEST EQUIPMENT

A	K
B	L
C	M
D	N
E	P
F	Q
G	R
H	S
J	T

Figure 3.2 - Test Data for 132/25 flat packs and leadless chip carriers.

TEST DESCRIPTION:

180 Grid Eval.

Sec No.	INITIAL FINE LEAK	INITIAL GROSS LEAK	POST ACCELL. FINE LEAK	POST ACCELL. GROSS LEAK	POST MECH SHOCK FINE LEAK	POST MECH SHOCK GROSS LEAK	POST TEMP CYCLE FINE LEAK	POST TEMP CYCLE GROSS LEAK
Pin:								
1	1.9×10^{-8}	Pass	5.6×10^{-9}	Pass	1.2×10^{-8}	Fail	—	—
2	1.0×10^{-8}	Pass	4.4×10^{-9}	Pass	1.9×10^{-8}	Canted	—	—
3	1.8×10^{-8}	Pass	7.6×10^{-9}	Pass	1.9×10^{-8}	Pass	1.6×10^{-8}	Pass
4	1.6×10^{-8}	Pass	8.8×10^{-9}	Pass	1.6×10^{-8}	Pass	1.8×10^{-8}	Pass
5	1.3×10^{-8}	Pass	9.6×10^{-9}	Pass	1.6×10^{-8}	Pass	1.8×10^{-8}	Pass
Pad:								
6	8.6×10^{-9}	Pass	3.6×10^{-9}	Pass	3.2×10^{-9}	Pass	3.6×10^{-9}	Pass
7	8.6×10^{-9}	Pass	3.6×10^{-9}	Pass	3.8×10^{-9}	Pass	3.8×10^{-9}	Pass
8	8.4×10^{-9}	Pass	3.6×10^{-9}	Pass	3.8×10^{-9}	Pass	3.8×10^{-9}	Pass
9	8.6×10^{-9}	Pass	3.6×10^{-9}	Pass	3.4×10^{-9}	Pass	3.6×10^{-9}	Pass
10	8.7×10^{-9}	Pass	3.6×10^{-9}	Pass	3.6×10^{-9}	Pass	3.6×10^{-9}	Pass

TEST COMMENTS:

ACCELL., 30,000 Gs Y1 _____ 1-10-85

MECH. SHOCK, 1,500 Gs .5 MIL. SEC. Y1 _____ 1-10-85

TEMP. CYCLE, -65 +150 10 CYCLES _____ 1-15-85

VISUAL:

POST ACCELL. _____ 1-11-85

POST MECH. SHOCK _____ 1-11-85

POST TEMP. CYCLE _____ 1-15-85

INITIAL: _____

DATE: _____

TEMP. _____

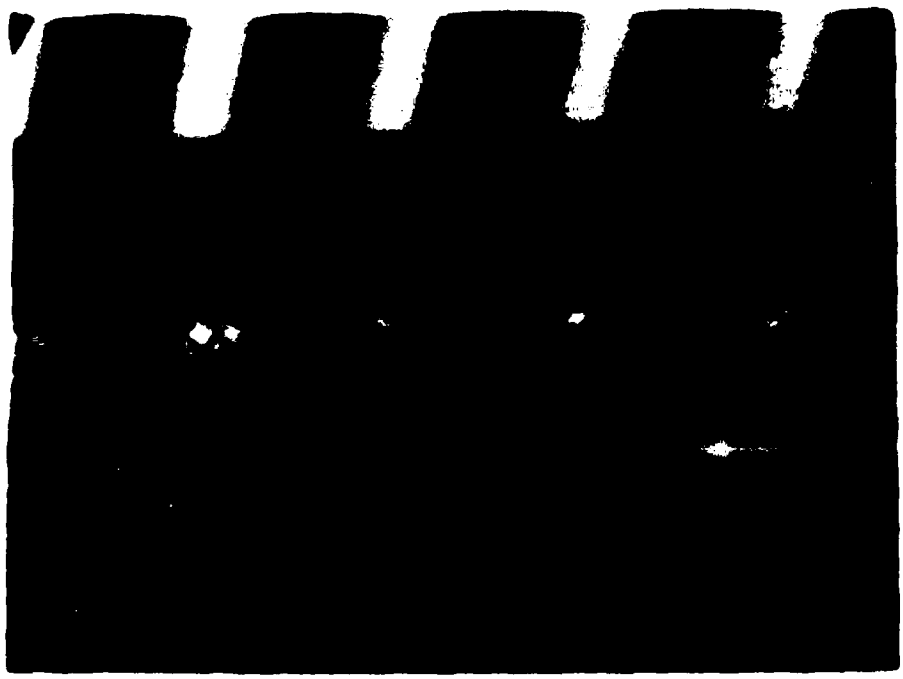
HUMIDITY: _____

CHECKED BY: _____

TEST EQUIPMENT:

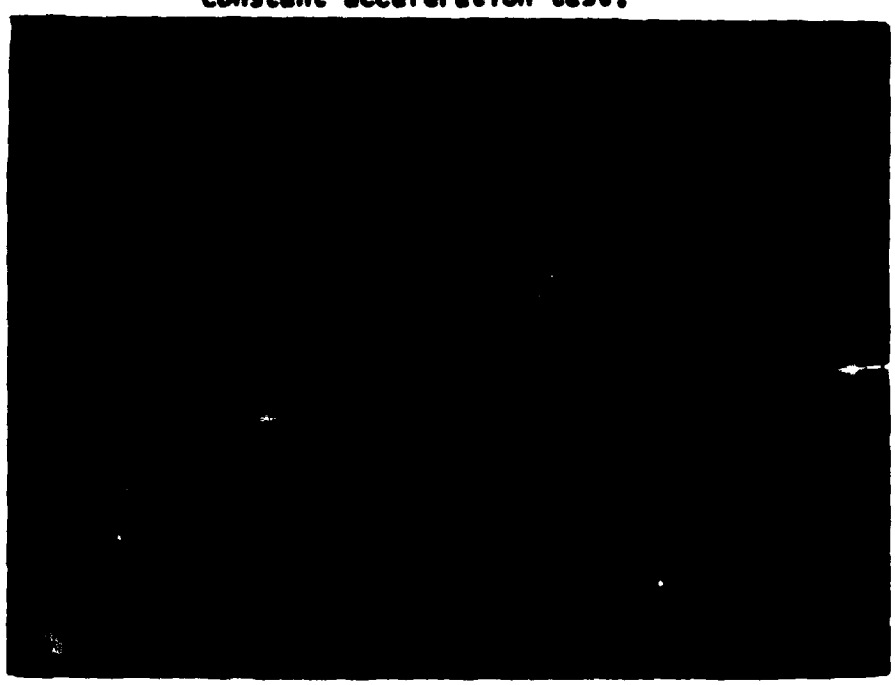
A	K
B	L
C	M
D	N
E	P
F	Q
G	R
H	S
J	T

Figure 3.3 - Test Data for 180 I/O pin- and pad-grid array packages.



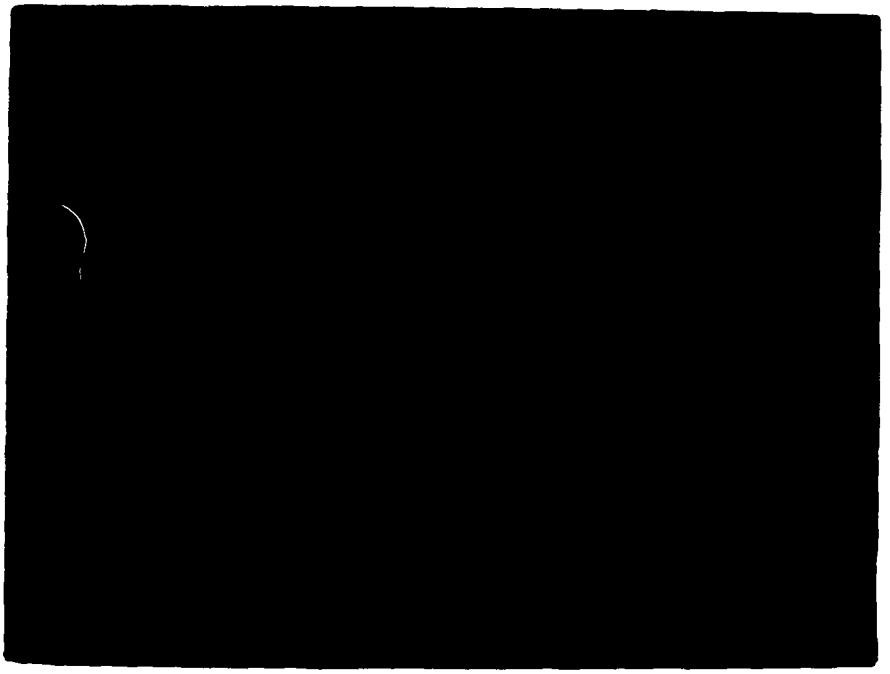
MAG: 50X

Figure 3.4 - Crack in glass seal in 132/25 flat pack following constant acceleration test.



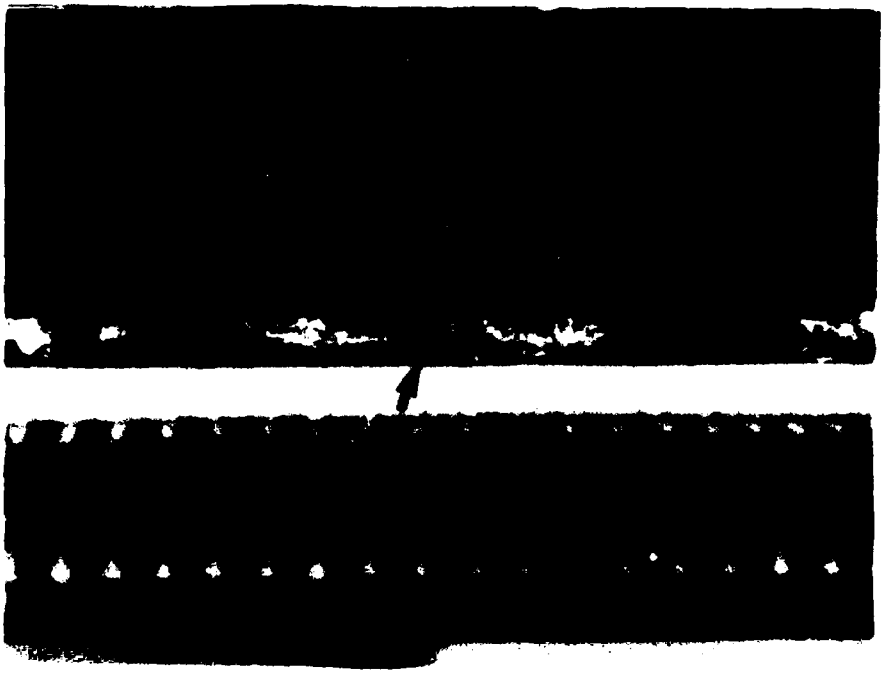
MAG: 20X

Figure 3.5 - Ultra-violet photograph of Zyglo escaping from crack in glass seal (dye penetrant test).



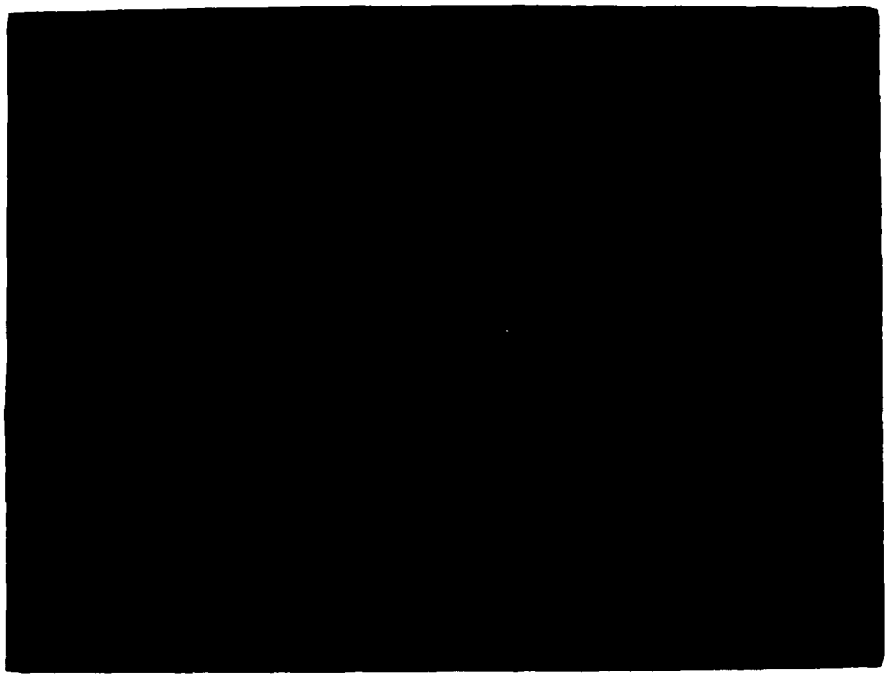
MAG: 3X

Figure 3.6(a) - Photograph of dye penetrant test showing leaks in the solder lid seal of a leadless chip carrier.



MAG: 10X

Figure 3.6(b) - Photograph showing one hole in the solder lid seal of the same package.

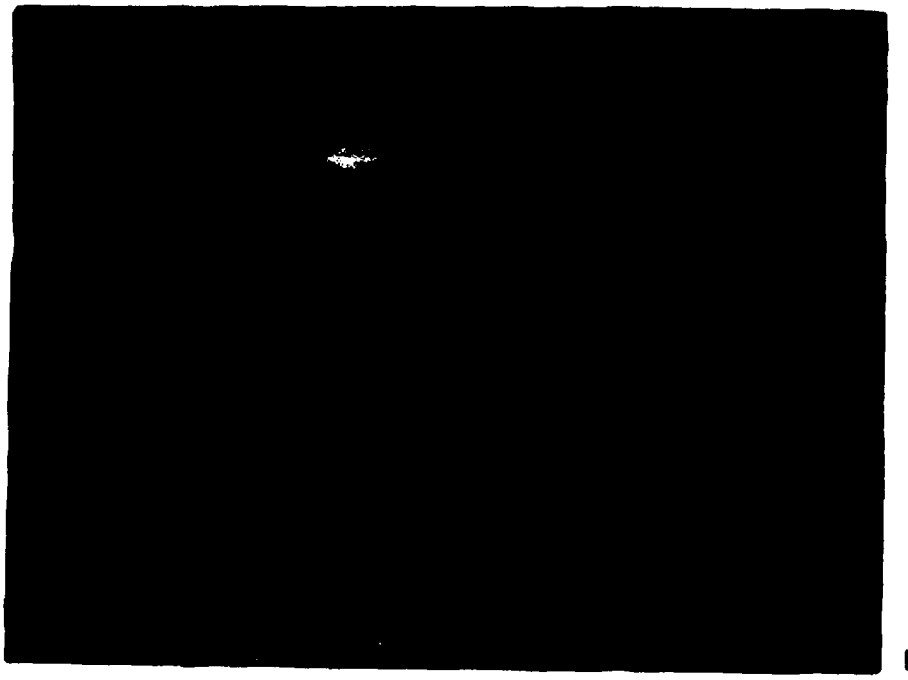


MAG: 3X

Figure 3.7(a) - Photograph of dye penetrant test showing gross leakage in the solder lid seal of a leadless chip carrier.

MAG: 10X

Figure 3.7(b) - Photograph showing leak site in the solder lid seal of the same package.

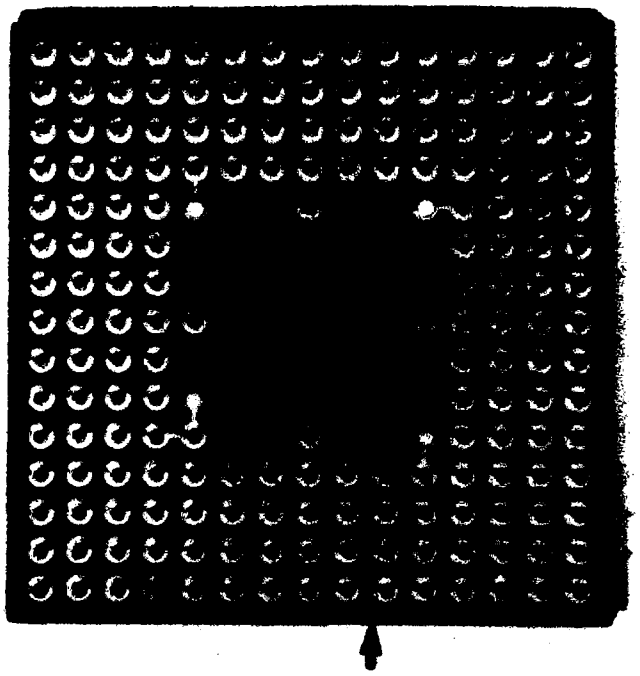


MAG: 2X

Figure 3.8(a) - Photograph of dye penetrant test showing leak sites in the solder lid seal of a 180 I/O pin grid array.

MAG: 10X

Figure 3.8(b) - Photograph showing absence of solder in the lid seal of the same package.



MAG: 2X

Figure 3.9(a) - Photograph showing fracture of 180 I/O pin-grid array package after Mechanical Shock test.

MAG: 2X

Figure 3.9(b) - Dye penetrant photograph of same package revealing finer cracks.

MAG: 2X

Figure 3.9(c) - Top side photograph of dye penetrant test of the same package showing that the cracks extend to the top of the package. Note also the leaks in the solder lid seal.

There were no difficulties in performing the Mechanical Shock test method, although fixturing was possibly a problem. Four parts failed hermeticity after this test: three from lid seal failures, and one from a combination of lid seal failure and cracked ceramic. The lid seal failures did not reflect on the test method itself, but on difficulties experienced during assembly. The cracked package, however, was probably from poor support to the package lid during test. Since most of the samples passed the test or failed for reasons not related to the test method, there is no reason to lower the maximum test limit (1500 g) for Method 2002. The one cracked package, however, illustrates the need for careful fixturing while performing this test.

RECOMMENDATIONS

No changes in the performance criteria of the four MIL-STD-883 tests considered here are recommended as a result of the test data obtained. It is possible to construct fixturing that will adequately support the package types considered here.

TASK 4: TERMINATION CHARACTERISTICS

OBJECT

To determine the impact of reduced terminal size and new terminal configurations on tests from MIL-STD-883 that are directly affected by terminal characteristics, i.e., Insulation Resistance (1003), Moisture Resistance (1004), Solderability (2003), and Lead Integrity (2004).

METHOD

Each test was performed to the present MIL-STD-883 method where possible. When problems were encountered, the conditions or limits were modified. Two new test methods were developed: Pin Grid Array Pull Test, and the Chip Carrier Push Test. The four test areas will be discussed separately in the following text.

Insulation Resistance

Method

Three packages of each of the six following configurations were tested: 24/50 flat pack, 132/25 flat pack, 132/25 leadless chip carrier, 144 I/O pad grid array, 180 I/O pin grid array, and 180 I/O pad grid array. All packages were made from ceramic.

The insulation resistance of each package was measured as follows: for all packages, the resistance was measured between three pairs of adjacent leads. One additional measurement was made on each package. For the flat packs the resistance was measured from every other lead removed from the lead frame and tied together, to the frame bar. For the four remaining package types, the resistance was measured from every termination tied together to the lid seal ring and die bonding pad tied together.

Each resistance measurement was made at eight different potentials: $\pm$10 V, $\pm$50 V, $\pm$100 V, $\pm$1000 V. The electrification time for each measurement was one minute.

Results

The data sheets for the entire test are included as Figures 4.1 through 4.6.

For the termination-pair measurements, only one measurement at $\pm$100 V or less (-670 nA at -100 V on a 132/25 leadless chip carrier) was above the maximum leakage current of 100 nA. The insulation resistance itself was 150 MΩ (1.5×10^8 ohm) which is ten times greater than the

PRODUCT ASSURANCE
MATERIALS AND COMPONENTS ENGINEERING AND TEST

TEST DESCRIPTION IR @ 10Vdc 50 vdc 100.vdc 1000.vdc

	PLUS					MINUS			
	10 v	50 v	100 v	1000 v		10 v	50 v	100 v	1000 v
1A	$.9 \times 10^{12}$	$.7 \times 10^{12}$	5×10^{11}	2×10^{11}	1A	1.6×10^{11}	$.3 \times 10^{12}$	$3. \times 10^{11}$	$2. \times 10^{11}$
2A	1.6×10^{11}	$.7 \times 10^{12}$	$3. \times 10^{11}$	$.9 \times 10^{11}$	2A	1.5×10^{11}	$.7 \times 10^{12}$	$5. \times 10^{11}$	3×10^{11}
3A	$4. \times 10^{11}$	1.4×10^{12}	$3. \times 10^{11}$	1.5×10^{10}	3A	3.0×10^{11}	2.4×10^{11}	$2. \times 10^{11}$	$4. \times 10^{11}$
1B	4.0×10^{11}	$.8 \times 10^{12}$	$.7 \times 10^{12}$	3.5×10^{11}	1B	$2. \times 10^{11}$	4×10^{11}	$4. \times 10^{11}$	$3. \times 10^{11}$
2B	1.6×10^{11}	$.7 \times 10^{12}$	$3. \times 10^{11}$	$.9 \times 10^{11}$	2B	1.5×10^{11}	$.7 \times 10^{12}$	$5. \times 10^{11}$	3.5×10^{11}
3B	$.8 \times 10^{12}$	$.6 \times 10^{12}$	$3. \times 10^{11}$	$4. \times 10^{11}$	3B	1.1×10^{11}	$.6 \times 10^{12}$	4.5×10^{11}	1.6×10^{11}

T COMMENTS:
SEE FIG 1 (NEXT PG) FOR HOOK-UP

INITIAL: ____
DATE: ____
TEMP. ____
HUMIDITY ____
CHECKED BY: ____

TEST EQUIPMENT

A	K
B	L
C	M
D	N
E	P
F	Q
G	R
H	S
J	T

Figure 4.1 - Insulation Resistance Data (lead-to-lead) for A) 24/50 flat pack, B) 132/25 flat pack.

PRODUCT ASSURANCE
MATERIALS AND COMPONENTS ENGINEERING AND TEST

	* PLUS					* MINUS			
	10V	50V	100V	1000V		10V	50V	100V	1000V
1A	1.5×10^{9}	$.67 \times 10^{12}$	2.9×10^{11}	3.5×10^{11}	1A	3×10^{12}	$.61 \times 10^{13}$	2.4×10^{12}	1.2×10^{12}
2A	$.97 \times 10^{11}$	1.9×10^{11}	2.6×10^{10}	3×10^{10}	2A	1.2×10^{11}	1.2×10^{11}	2.1×10^{9}	2.2×10^{10}
3A	2.7×10^{11}	1.5×10^{10}	1.5×10^{10}	1.2×10^{10}	3A	3.4×10^{11}	$.7 \times 10^{13}$	2.6×10^{10}	2.6×10^{10}
1B	1×10^{7}				1B	1×10^{7}			
2B	$< .5 \times 10^{6}$				2B	$< .5 \times 10^{6}$			
3B	$< .5 \times 10^{6}$				3B	$< .5 \times 10^{6}$			

TEST COMMENTS:

* PLUS = FRAME BAR NEGATIVE
MINUS = FRAME BAR POSITIVE

MEASURED FROM EVERY OTHER LEAD REMOVED FROM FRAME BAR & TIED TOGETHER TO FRAME BAR

INITIAL: OC
DATE:
TEMP. RA
HUMIDITY:
CHECKED BY:

TEST EQUIPMENT

A	K
B	L
C	M
D	N
E	P
F	Q
G	R
H	S
J	T

Figure 4.2 - Insulation Resistance Data (terminations-to-case) for A) 24/50 flat pack, B) 132/25 flat pack.

PRODUCT ASSURANCE
MATERIALS AND COMPONENTS ENGINEERING AND TEST

TEST DESCRIPTION: I_R @ 10VDC, 50VDC, 100VDC, 1000VDC

	PLUS					MINUS			
	10V	50V	100V	1000V		10V	50V	100 V	1000V
* 1C	$1.6X10^{11}$	$3.5X10^{11}$	$1.5X10^{8}$	$1.6X10^{11}$	1C	$2.1X10^{11}$	$2.2X10^{8}$	$.75X10^{8}$	$6.6X10^{11}$
2C	$3.5X10^{11}$	$2.5X10^{11}$	$2.5X10^{11}$	$1.5X10^{4}$	2C	$3X10^{11}$	$2.5X10^{11}$	$2.4X10^{8}$	$1.5X10^{9}$
3C	$2.5X10^{11}$	$2.5X10^{11}$	$1X10^{11}$	$2.1X10^{11}$	3C	$2.9X10^{8}$	$2.5X10^{8}$	$1X10^{11}$	$2X10^{8}$
	PINS	2 TO PIN 3					PIN 2 TO PIN 3		
Δ 1C	$1.6X10^{8}$	$2.4X10^{8}$	$1.8X10^{10}$	$2.1X10^{10}$	1C	$1.7X10^{10}$	$5X10^{10}$	$1X10^{10}$	$1X10^{10}$
2C	$5X10^{11}$	$3.8X10^{11}$	$1.1X10^{11}$	$2.4X10^{8}$	2C	$3X10^{11}$	$1.4X10^{11}$	$3X10^{8}$	$1.1X10^{4}$
3C	$5X10^{12}$	$5X10^{12}$	$1.5X10^{12}$	SHORT	2C	$3X10^{9}$	$1X10^{9}$	$1.5X10^{9}$	SHORT
	PIN	32 TO PIN 33					PIN 32 TO	PIN 33	
1C	$1.5X10^{10}$	$.45X10^{11}$	$.6X10^{11}$	$.9X10^{11}$	1C	$1.5X10^{11}$	$.7X10^{11}$	$.9X10^{11}$	$1.4X10^{4}$
2C	$1.5X10^{10}$	$.65X10^{8}$	$1.2X10^{11}$	SHORT	2C	$1.2X10^{10}$	$.45X10^{11}$	$3X10^{10}$	SHORT
3C	$1.2X10^{10}$	$.56X10^{11}$	$.8X10^{11}$	SHORT	3C	$.9X10^{10}$	$.4X10^{8}$	$.62X10^{8}$	SHORT
		PINS TO PIN 66					PIN 65 TO	PIN 66	
1C	$1.9X10^{4}$	$.5X10^{11}$	$.8X10^{11}$	$1.5X10^{11}$	1C	$.8X10^{10}$	$.4X10^{11}$	$2X10^{10}$	$.8X10^{4}$
2C	$1.3X10^{10}$	$.55X10^{4}$	$1X10^{11}$	$1.5X10^{11}$	2C	$1.1X10^{10}$	$.45X10^{8}$	$.7X10^{11}$	$1.3X10^{11}$
3C	$1.2X10^{10}$	$.45X10^{11}$	$.9X10^{11}$	SHORT	3C	$1X10^{10}$	$.45X10^{11}$	$.8X10^{11}$	SHORT

TEST COMMENTS:

* ALL LEADS TIED TOGETHER TO LID BONDING AREA
TIED TO CHIP BONDING AREA
PLUS = LEADS POSITIVE
MINUS = LEADS NEGATIVE

Δ BETWEEN ADJACENT PAIRS
POSITIVE = LOWER NUMBER PIN IN PAIR
NEGATIVE = " " " " "

INITIAL: JC
DATE:
TEMP: RA
HUMIDITY:
CHECKED BY:

TEST EQUIPMENT

A	K
B	L
C	M
D	N
F	P
F	Q
G	R
H	S
J	T

Figure 4.3 - Insulation Resistance Data (complete) for 132/25 leadless chip carrier.

PRODUCT ASSURANCE
MATERIALS AND COMPONENTS ENGINEERING AND TEST

TEST DESCRIPTION: IR @ 10V, 50VDC, 100VDC, 1000VDC

		* PLUS					* MINUS				
		10V	50V	100V	1000V			10V	50V	100V	1000V
*	1D	3.5×10^{11}	1.5×10^{12}	2×10^{12}	1.5×10^{10}		1D	2.5×10^{10}	1.1×10^{11}	2.2×10^{11}	5×10^{11}
	2D	$.9 \times 10^{11}$	$.7 \times 10^{11}$	$.8 \times 10^{11}$	2.5×10^{11}		2D	1.6×10^{10}	$.5 \times 10^{11}$	3.3×10^{10}	SHORTED
	3D	$.9 \times 10^{11}$	$.6 \times 10^{11}$	$.7 \times 10^{11}$	SHORT		3D	$.9 \times 10^{11}$	$.7 \times 10^{11}$	3×10^{10}	SHORT
		"A" POS						"A" NEG			
ANOS A+B	1D	1×10^{10}	1.9×10^{10}	$.7 \times 10^{10}$	$.63 \times 10^{10}$		1D	1×10^{10}	1.5×10^{10}	1.3×10^{10}	1.5×10^{10}
	2D	1.8×10^{10}	$.65 \times 10^{10}$	1.6×10^{10}	$.58 \times 10^{10}$		2D	$.95 \times 10^{10}$	1.5×10^{10}	1.3×10^{10}	1.4×10^{10}
	3D	1×10^{10}	$.9 \times 10^{10}$	1×10^{10}	1.2×10^{10}		3D	1×10^{10}	1×10^{10}	1.3×10^{10}	$.9 \times 10^{10}$
		"C" POS						"C" NEG			
BIAS CAP	1D	1.6×10^{12}	2.3×10^{11}	2.4×10^{10}	3.8×10^{10}		1D	3.4×10^{10}	3.5×10^{10}	$.75 \times 10^{11}$	$.9 \times 10^{11}$
	2D	3.2×10^{10}	$.7 \times 10^{11}$	2.2×10^{10}	3.0×10^{10}		2D	3.6×10^{10}	$.8 \times 10^{11}$	$.45 \times 10^{10}$	$.6 \times 10^{11}$
	3D	1.7×10^{10}	4×10^{10}	2.3×10^{10}	2.8×10^{10}		3D	3.5×10^{10}	5.2×10^{10}	3.0×10^{10}	1.6×10^{8}
		"E" POS						"E" NEG			
ANOS GND	1D	$.62 \times 10^{9}$	1.9×10^{11}	$.6 \times 10^{9}$	$.7 \times 10^{9}$		1D	3.0×10^{10}	1.6×10^{11}	$.7 \times 10^{9}$	$.8 \times 10^{11}$
	2D	1.2×10^{9}	1.5×10^{9}	$.9 \times 10^{9}$	1.6×10^{11}		2D	$.56 \times 10^{9}$	1.2×10^{11}	$.65 \times 10^{9}$	$.85 \times 10^{11}$
	3D	1.6×10^{9}	1.4×10^{11}	1.2×10^{11}	3.0×10^{9}		3D	$.6 \times 10^{11}$	1.5×10^{11}	$.9 \times 10^{11}$	$.75 \times 10^{11}$

TEST COMMENTS:

* PLUS = LEADS POSITIVE
MINUS = LEADS NEGATIVE
MEASUREMENT TAKEN FROM ALL LEADS TIED TOGETHER TO LID BONDING AREA TIED TO CHIP BONDING AREA

INITIAL: [illegible]
DATE: [illegible]
TEMP: [illegible]
HUMIDITY: ____
CHECKED BY: ____

TEST EQUIPMENT

A ✓	K
B	L
C	M
D	N
E	P
F	Q
G	R
H	S
J	T

Figure 4.4 - Insulation Resistance Data (complete) for 144 I/O pad grid array.

PRODUCT ASSURANCE
MATERIALS AND COMPONENTS ENGINEERING AND TEST

TEST DESCRIPTION: 180 Pin Grid Array

Insulation Resistance @ Plus & minus 10 V, 50 V, 100 V, 1000 V

Lead to case	Plus 10 V	Plus 50 V	Plus 100 V	Plus 1000 V	minus 10 V	minus 50 V	minus 100 V	minus 1000 V
1-E	1.6×10^{10}	1.2×10^{10}	1.1×10^{10}	1.2×10^{10}	1.4×10^{10}	1.6×10^{10}	1.4×10^{10}	1.0×10^{10}
2-E	7.5×10^{10}	4.8×10^{10}	5.5×10^{10}	6.6×10^{10}	1.6×10^{10}	4.6×10^{10}	6.2×10^{10}	3.2×10^{10}
3-E	2.6×10^{10}	6.5×10^{10}	7.5×10^{10}	8.0×10^{10}	2.5×10^{10}	7.5×10^{10}	10.6×10^{10}	7.5×10^{10}
Pin to TAB 1-E	2.4×10^{11}	3.6×10^{11}	2.6×10^{11}	3.0×10^{11}	1.7×10^{11}	3.6×10^{11}	3.5×10^{11}	2.9×10^{11}
2-E	3.0×10^{11}	3.2×10^{11}	3.0×10^{11}	2.5×10^{11}	2.0×10^{11}	3.0×10^{11}	3.5×10^{11}	2.8×10^{11}
3-E	1.0×10^{11}	3.8×10^{11}	3.5×10^{11}	2.6×10^{11}	2.2×10^{11}	4.0×10^{11}	4.0×10^{11}	3.5×10^{11}
Pin to ELEMENT 1-E	4.0×10^{11}	4.1×10^{11}	4.0×10^{11}	3.5×10^{11}	2.9×10^{11}	3.6×10^{11}	3.5×10^{11}	3.0×10^{11}
2-E	6.8×10^{11}	6.0×10^{11}	6.0×10^{11}	6.0×10^{11}	3.0×10^{11}	5.2×10^{11}	5.4×10^{11}	4.5×10^{11}
3-E	6.1×10^{11}	5.3×10^{11}	5.1×10^{11}	4.0×10^{11}	4.5×10^{11}	4.4×10^{11}	4.5×10^{11}	3.0×10^{11}
Pin to GLASS 1-E	4.5×10^{11}	4.4×10^{11}	4.5×10^{11}	3.5×10^{11}	2.4×10^{11}	3.5×10^{11}	3.5×10^{11}	3.0×10^{11}
2-E	4.5×10^{11}	4.2×10^{11}	4.0×10^{11}	3.4×10^{11}	2.2×10^{11}	4.4×10^{11}	4.5×10^{11}	4.0×10^{11}
3-E	6.6×10^{11}	5.4×10^{11}	5.3×10^{11}	4.3×10^{11}	2.1×10^{11}	4.1×10^{11}	4.5×10^{11}	4.0×10^{11}

TEST COMMENTS

INITIAL	[illegible]
DATE	9-7-84
TEMP	Rac
HUMIDITY	Acb
CHECKED BY	

TEST EQUIPMENT

A	K
B	L
C	M
D	N
E	P
F	Q
G	R
H	S
J	T

Figure 4.5 - Insulation Resistance Data (complete) for 180 I/O pin grid array.

TEST DESCRIPTION INSULATION RESISTANCE
PAD GRID ARRAY
180 LEADS

		* POS.				* NEG			
		10 V	50 V	100 V	1,000 V	10 V	50 V	100 V	1 000 V
PINS TO CASE	1F	5 x 10^{11}	6 x 10^{11}	4 x 10^{11}	3 x 10^{11}	1 x 10^{11}	.3 x 10^{12}	4 x 10^{11}	3 x 10^{11}
	2F	5 x 10^{11}	.8 x 10^{12}	.7 x 10^{12}	3 x 10^{11}	2 x 10^{11}	.4 x 10^{12}	5 x 10^{11}	4 x 10^{11}
	3F	6 x 10^{11}	.6 x 10^{12}	5 x 10^{11}	3 x 10^{11}	1 x 10^{11}	2 x 10^{11}	3 x 10^{11}	1.3 x 10^{11}
PADS A B	1F	1.2 x 10^{10}	3 x 10^{10}	.7 x 10^{10}	.6 x 10^{10}	3 x 10^{9}	.5 x 10^{10}	4 x 10^{9}	3.5 x 10^{9}
	2F	6 x 10^{9}	1 x 10^{10}	5 x 10^{9}	4 x 10^{9}	3 x 10^{9}	5 x 10^{9}	4 x 10^{9}	3 x 10^{9}
	3F	.7 x 10^{10}	5 x 10^{9}	1.5 x 10^{9}	SHORT	— —	— —	— —	— —
C D	1F	.8 x 10^{11}	1.5 x 10^{10}	.6 x 10^{10}	.6 x 10^{10}	3 x 10^{9}	.4 x 10^{10}	5 x 10^{9}	4.5 x 10^{9}
	2F	.7 x 10^{10}	.6 x 10^{10}	.6 x 10^{10}	.65 x 10^{10}	3 x 10^{9}	.6 x 10^{10}	3 x 10^{9}	4 x 10^{9}
	3F	1 x 10^{10}	1.5 x 10^{10}	.7 x 10^{10}	.75 x 10^{10}	5 x 10^{9}	1 x 10^{10}	4 x 10^{9}	5 x 10^{9}
E F	1F	5 x 10^{9}	.4 x 10^{10}	.3 x 10^{9}	4 x 10^{9}	4 x 10^{9}	.8 x 10^{10}	4 x 10^{9}	4.5 x 10^{9}
	2F	1 x 10^{10}	1.2 x 10^{10}	.8 x 10^{10}	3 x 10^{9}	4 x 10^{9}	5 x 10^{9}	4 x 10^{9}	3 x 10^{9}
	3F	.7 x 10^{10}	.75 x 10^{10}	.7 x 10^{10}	.8 x 10^{10}	4 x 10^{9}	5 x 10^{9}	5 x 10^{9}	3.5 x 10^{9}

TEST COMMENTS

* POS = A, C, E POSITIVE

* NEG = A, C, E NEGATIVE

INITIAL	SS
DATE	8/13/-
TEMP	R.A.C
HUMIDITY	R.A.C
CHECKED BY	

TEST EQUIPMENT

A	✓	K	
B		L	
C		M	
D		N	
E		P	
F		Q	
G		R	
H		S	
J		T	

Figure 4.6 - Insulation Resistance Data (complete) for 180 I/O pad grid arrays.

minimum insulation resistance. Several failures (near short conditions) were noted at ±1000 V, however. Two 132/25 leadless chip carriers and one 180 I/O pad-grid array showed shorts between terminations at ±1000 V.

Two package types failed the all-leads-to-case measurements. Two 144 I/O pad-grid arrays shorted at ±1000 V. Also, all three 132/25 flat packs measured below 15 MΩ resistance at all voltages.

Conclusions

From the test data, it appears that ±1000 V applied voltage exceeds the capabilities of some high I/O packages. The packages tested had no difficulty withstanding the ±100 V applied voltage (test condition D) which is commonly used. A limit of ±100 V is therefore recommended, although the maximum applied voltage was not determined for these packages. In any case, the method was adequate for performance of these measurements.

Moisture Resistance

Method

Moisture Resistance was performed, according to MIL-STD-883, Method 1004, on four package types. Five packages each of the following were tested: 24/50 flat pack, 132/25 flat pack, 132/25 leadless chip carrier, and 180 I/O pin grid array.

Initial conditioning, in accordance with Method 2004, Test Condition B_1 (Bending Stress) was performed on the two leaded devices. Ten pairs of adjacent leads or chip carrier terminals were selected for testing. The insulation resistance between these lead pairs was measured per Method 1003 at 100 V_{DC} before exposure to moisture, and after each 10-cycle interval. A polarizing voltage of 100 V_{DC} was placed across these pairs during the moisture-resistance cycle.

The packages were subjected to the sequence cycle shown in Figure 1004.1 of the test method. The test consisted of ten 24-hour cycles, each cycle containing two temperature excursions of +25°C to +65°C under 90 percent relative humidity. Five of the ten cycles also contained a cold cycle from +25°C to -10°C. Insulation resistance measurements and visual examination were made at 10-cycle intervals.

Results

A sample data sheet of results is shown as Figure 4.7. All parts passed 10 cycles of test. Data were recorded individually after failures occurred. These failures are summarized below in Table 4.1

TABLE 4.1 - SUMMARY OF MOISTURE RESISTANCE PACKAGE FAILURES

Package Style	No. of Package Failures				
	After 10 Cycles	After 20 Cycles	After 30 Cycles	After 40 Cycles	Total
24/50 Flat pack	0	0	0	0	0
132/25 Flat pack	0	0	1	N/A	1
132/25 Leadless CC	0	1	0	4	5
180 I/O Pin Grid Array	0	4	0	1	5

TEST DESCRIPTION: INSULATION RESISTANCE/@ MOISTURE RESISTANCE

S/N 3C	COMMON / PIN #	ROOM TEMP INITIAL	POST 20 CYCLES	POST 30 CYCLES	POST 40 CYCLES			
A	44 / 43	5.0×10^{11}	Ok	OK	—	✓		
	46 / 45	5.0×10^{11}	↓	↓	1.5×10^{9}			
	48 / 47	5.0×10^{11}			2.0×10^{9}			
	50 / 49	5.0×10^{11}			—	✓		
	52 / 51	5.0×10^{11}			—	✓		
B	114 / 115	4.0×10^{11}	6.0×10^{9}		3.0×10^{9}			
	116 / 117	4.5×10^{11}	1.6×10^{10}		$.7 \times 10^{10}$			
	118 / 119	3.0×10^{11}	1.3×10^{10}		1.5×10^{10}			
	120 / 121	3.5×10^{11}	1.4×10^{10}		2.0×10^{10}			
	122 / 123	3.5×10^{11}	10×10^{9}	↓	1.0×10^{10}			
TECH		SS	SS	SS	SS			
DATE		10-25-85	11-26-85	12-9-85	2-28-86			

TEST COMMENTS

INITIAL	SS
DATE	12/31
TEMP	
HUMIDITY	
CHECKED BY	

TEST EQUIPMENT

A	K
B	L
C	M
D	N
E	P
F	Q
G	R ✓
H	S
J	T

Figure 4.7 - Sample Moisture Resistance Data Sheet.

In this table, one failing termination pair was considered a package failure. A package failure was counted only at the first time a failure was detected. The 132/50 flat packs were not subjected to testing beyond 30 cycles. The entire test was terminated when 10 failures occurred as this represented 50 percent failures for the group of 20 test samples.

Conclusions

The present Moisture Resistance test (Method 1004) can be applied to packages with lead spacings of 25 mil and 50 mil separations. The packages tested here passed Insulation Resistance after 10 cycles which is the standard test duration. Apparently the 180 I/O pin grid array configuration was the most susceptible to moisture and the 24/50 flat pack the least.

Solderability

Method

The method used was exactly as specified by MIL-STD-883C, Method 2003.3, with the following exception: a bake-out sequence designed to simulate the die-attach and lid seal process temperatures was performed on all of the test packages. The bake-out sequence was:

1) 10 min. @ 250°C

2) 20 - 25 sec @ 450°C

3) 10 min. @ 250°C

   - To simulate gold-silicon die attach.

4) 25 min. cycle starting at ambient temp., peaking at 350°C, then cooling to ambient.

   - To simulate travel through a soldering oven (lid seal).

The packages used were chosen for this test because of fine termination spacing and anticipated difficulties in soldering. They were: 24/50 flat pack, 132/25 flat pack, 132/25 leadless chip carrier, 144 I/O pad grid array, 180 I/O pad grid array, and 180 I/O pin grid array. Four packages of each type were tested.

All packages were dipped into the solder pot at an angle of approximately 30 degrees from the horizontal.

Results

All of the leaded packages passed the MIL-STD-883C requirements for solderability as written. Figure 4.8 is an example of a 24/50 flat pack after soldering; Figure 4.9 a 132/25 flat pack; Figure 4.10 a 180 I/O pin grid array. The right and bottom sides were inadvertantly dipped into a pot containing slightly contaminated solder. The solder in the pot was replaced, and the top set of leads was then dipped. The figure shows good coverage of these leads. The solder bridging of the end leads of the top row was caused by deformation from cutting the lead frame, and is not a package failure.

The 132/25 leadless chip carriers also passed the test, as shown in Figure 4.11. The left side was dipped into the contaminated pot, the bottom side in new solder, which covered adequately.

Difficulty was experienced in soldering the pad grid array packages. Figure 4.12 illustrates the problem. The top side of the 180 I/O pad grid array shows the results of a single 5-sec. dip in the solder pot. The bottom side is the result of an immediate second 5-sec. dip in the solder pot (no additional flux applied). This produced excellent coverage of every pad. Figure 4.13 shows good results on a double-dipped 144 I/O pad grid array.

To determine whether the bake-out process affected the gold braze pads, baked and unbaked samples of 180 I/O pad grid arrays were cross-sectioned and examined. No significant difference in plating layer thicknesses nor degradation of the gold layer was detected, either visually or by EDS X-ray spectroscopy.

Apparently the high thermal mass of the pad grid array package combined with the large pad size prevented the pad from uniformly reaching soldering temperature ($\sim$185°C) during the 5-sec. dwell in the 245°C solder pot.

Conclusions

Method 2003 of MIL-STD-883C appears to be an adequate test of the solderability of flat packs and leadless chip carriers, based on the results of this study.

The 144- and 180-I/O pad grid arrays tested were not able to pass the existing test. The dwell time in the solder pot should be increased from 5-sec. to 10-sec. maximum. This change is noted in the test methods section of the Appendix.

Finally, the bake-out procedure produced no degradation in the performance of these packages.

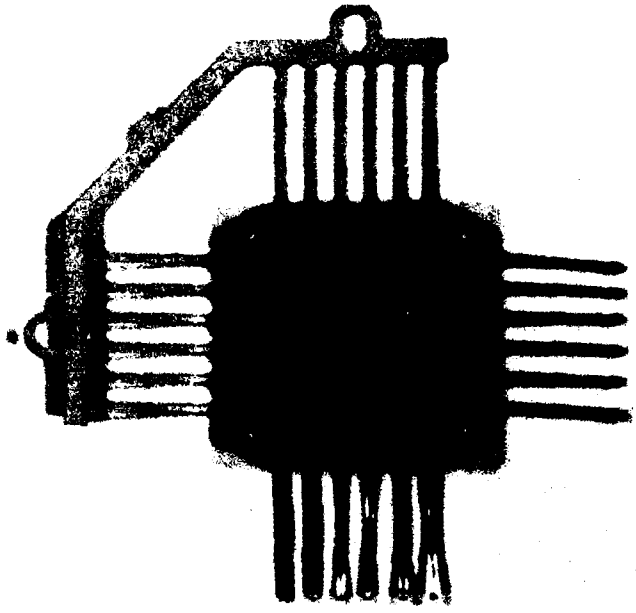


Figure 4.8 - 24/50 flat pack showing good solderability.

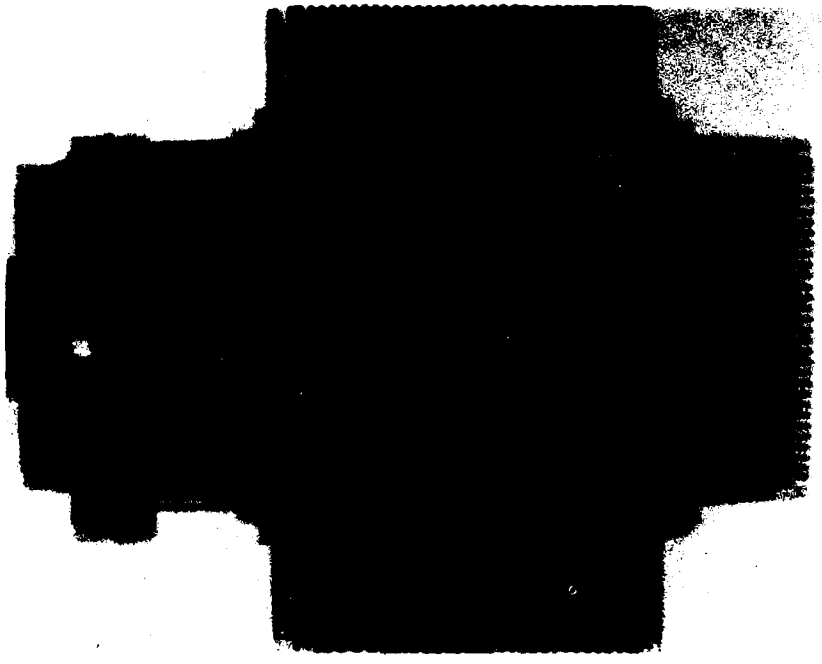


Figure 4.9 - 132/25 flat pack following testing. Right and bottom sets of leads dipped in contaminated solder. Top set dipped in new solder shows good coverage. Note: solder bridging is due only to lead bending.

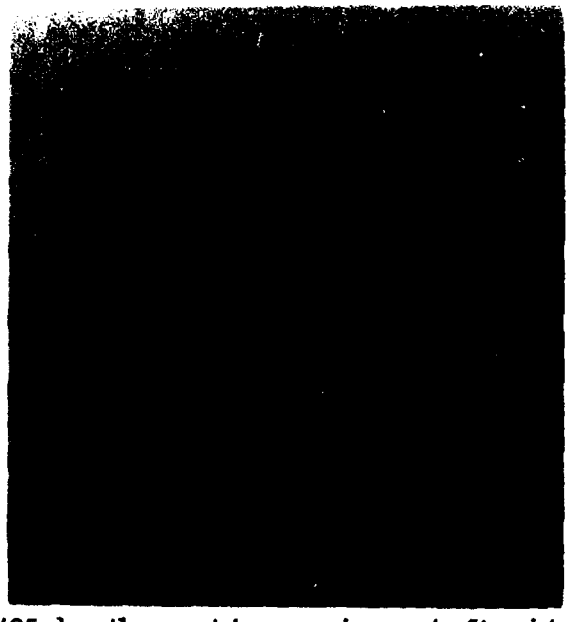


Figure 4.10 - 132/25 leadless chip carrier. Left side dipped in contaminated solder, bottom in new solder.

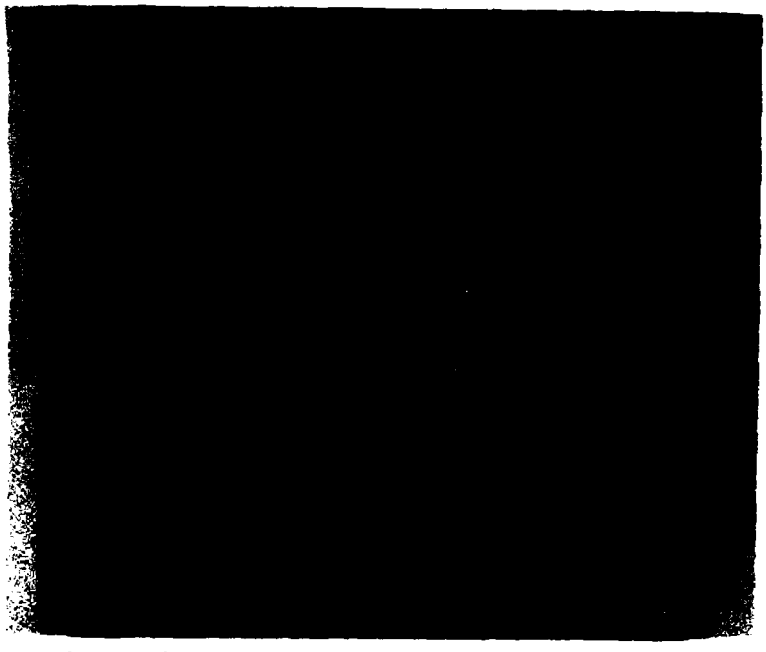


Figure 4.11 - A 180 I/O pad grid array following testing. Top rows show poor wetting from a single dipping. Bottom rows show excellent wetting for a second dipping in the solder.

Figure 4.12 - A 180 I/O pin grid array following solderability tests. All pins showed excellent wetting.

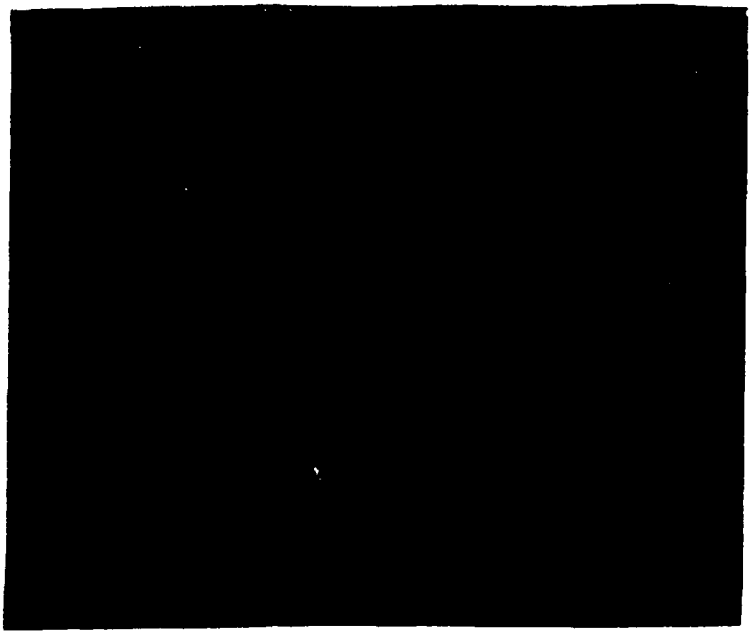


Figure 4.13 - A 144 I/O pad grid array following testing. All pads were double-dipped and show excellent wetting.

Lead Integrity

Method

Three different test methods were used on the test packages. For the 24/50 and 132/25 flat packs, MIL-STD-883, Method 2004, Condition B2 (lead fatigue) was performed exactly as specified. The leads of both package types had a cross section of less than 0.006 x 0.020 in. and were tested with a force of 3 ounces. Five packages of each type were tested in this way. Ten leads on each package were tested.

According to the above test method, the 180 I/O pin grid array samples would be tested with the same bending force (3 oz.) used above, since they have leads with a diameter of 0.018 in. This load does not adequately test the strength of either the lead or its attachment to the braze pad. As an alternative, a lead pull test was developed. A Dage MCT-15 microtester with a tweezer attachment was used to grasp the lead and pull it (with the package held fixed) perpendicularly away from the package. Leads from two 180 I/O pin grid array packages were tested in this way.

A chip carrier push test was developed to assess the "lead integrity" of leadless chip carriers. Boards mounted with chip carriers were drilled from behind to the back of each chip carrier. The board was then mounted onto a 1/2 in. thick steel plate (having the same hole pattern as the board) with epoxy. The board was also bolted to the plate at the corners. A steel post of appropriate diameter (slightly smaller than the hole) was then used to push the chip carrier off the board using an Instron tester. Teflon tape was inserted between the post and the carrier to insure even application of the pushing force.

To evaluate the effectiveness of this test, sample boards were prepared by drilling behind the chip carriers and mounting onto a steel backing plate. Joints on 23 chip carriers were checked for electrical continuity by probing between the package and board. The sample was then temperature cycled from -55°C to +125°C per MIL-STD-883, Method 1010. Interim measurements were performed at 20-cycle increments until a total of 60 cycles was reached.

Finite element modelling was used to predict trends for larger packages. These results were analyzed and used to set the recommended test limit.

Results

Flat Packs

The data sheets for the 24/50 and 132/25 flat packs are included as Figures 4.14 and 4.15, respectively. The dimensions of the leads were:

24/50	0.11 x 0.010 in.
132/25	0.013 x 0.006 in.

As can be seen from the data sheets, no failures were observed on these packages.

Pin Grid Arrays

The data from pull testing leads from the pin grid array packages is shown in Table 4.2 (page 62). Seventy-four leads were pulled from two packages. The mean pull strength was 6303 g-force with a standard deviation of 691 g-force. The pull strength distribution is shown in Figure 4.16. In all cases, the lead itself broke rather than detaching from the braze pad.

Leadless Chip Carriers

During development of the test method, the chip carriers were broken by the metal post. Adding teflon tape between the post and the ceramic base of the carrier solved this problem The push test setup is shown in Figure 4.17, and a photograph of a sample board after testing is included as Figure 4.18. Initial test measurements before the procedure was refined are shown in Table 4.3 below.

TABLE 4.3 - DEVELOPMENTAL CHIP CARRIER PUSH STRENGTHS

No. of Terminations on Chip Carrier	*Push Test (lb-Force)
20	84, 108, 86
28	132, 126, 143
44	250, 236, 212
64	331, 262, 270

*Test performed without tape.

TEST DESCRIPTION

LEAD INTEGRITY

DEVICE NO	Bend on Pin No.		Bend on Pin No.		Bend on Pin No.		Bend on Pin No.		Bend on Pin No.		Visual		
1	13	14	15	16	17	18	21	22	23	24	P		
2	3	4	5	6	7	8	9	10	11	12	P		
3	1	2	3	4	5	6	7	8	9	10	P		
4	1	2	3	4	5	6	7	8	9	10	P		
5	1	2	3	4	5	6	7	8	9	10	P		

Figure 4.14 - Data from lead fatigue test on 24/50 flat packs. All packages passed.

TEST DESCRIPTION

LEAD INTEGRITY

DEVICE No	Bend on Pin No.		Bend on Pin No.		Bend on Pin No.		Bend on Pin No.		Bend on Pin No.		VISUAL
1	1	2	3	12	13	14	23	31	32	33	P
3	4	5	6	11	12	13	14	26	27	28	P
4	3	4	5	6	12	13	14	27	28	29	P
5	1	2	9	10	21	22	23	29	30	33	P
6	7	8	9	10	20	21	22	29	30	31	P

Figure 4.15 - Data from lead fatigue test on 132/25 flat packs. All packages passed.

TABLE 4.2 - PIN GRID ARRAY LEAD PULL STRENGTHS

Lead #	Pull Strength (g-force)	Lead #	Pull Strength (g-force)
1	6500	38	6200
2	5850	39	4700
3	8150	40	7200
4	6150	41	6450
5	6150	42	6600
6	6300	43	6550
7	5200	44	7100
8	6350	45	7400
9	6050	46	6950
10	6000	47	7350
11	7400	48	7000
12	6350	49	6900
13	6250	50	7500
14	6450	51	6750
15	5900	52	6150
16	6100	53	7400
17	6200	54	5750
18	6500	55	5450
19	6600	56	6400
20	6450	57	6400
21	6350	58	6450
22	6250	59	6350
23	5850	60	6450
24	6050	61	6250
25	6200	62	6750
26	7750	63	6500
27	6750	64	6500
28	6650	65	6400
29	6250	66	6150
30	7750	67	5200
31	6150	68	5750
32	5900	69	6100
33	6250	70	4950
34	5100	71	5300
35	5500	72	4800
36	5350	73	5450
37	5400	74	6450

$n = 74$

$\bar{X} = 6303$ g-force

$\sigma = 691$ g-force

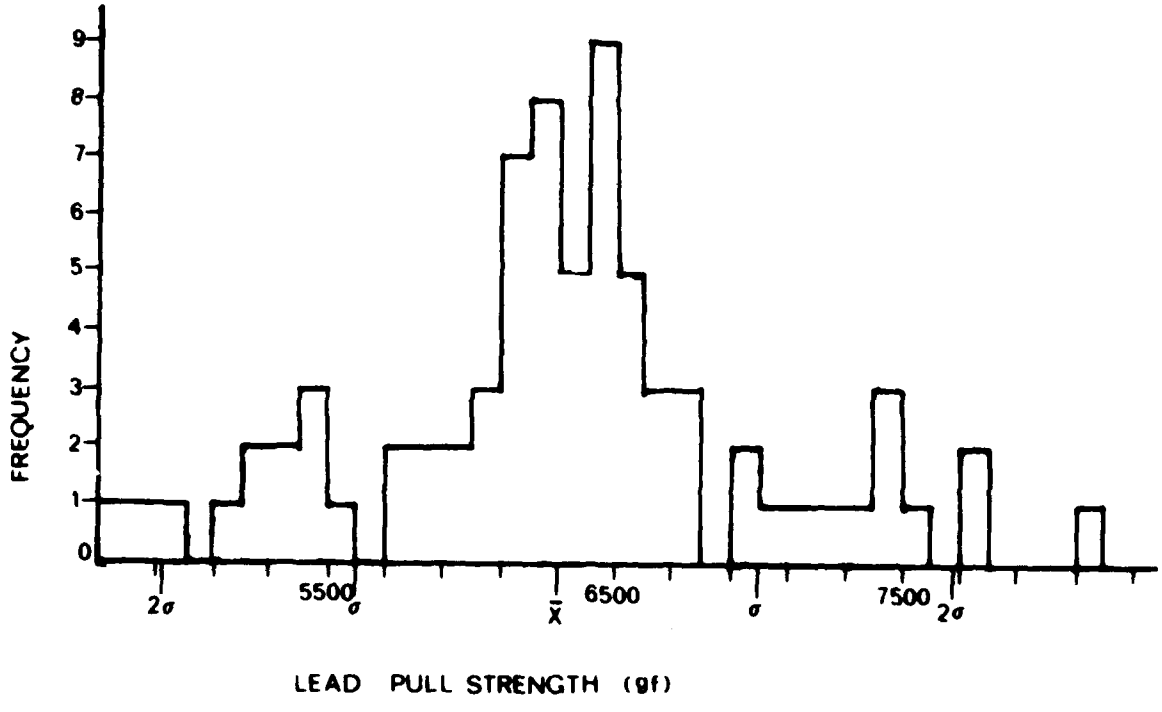


Figure 4.16 - 180 I/O Pin Grid Array Lead Pull Strength Distribution

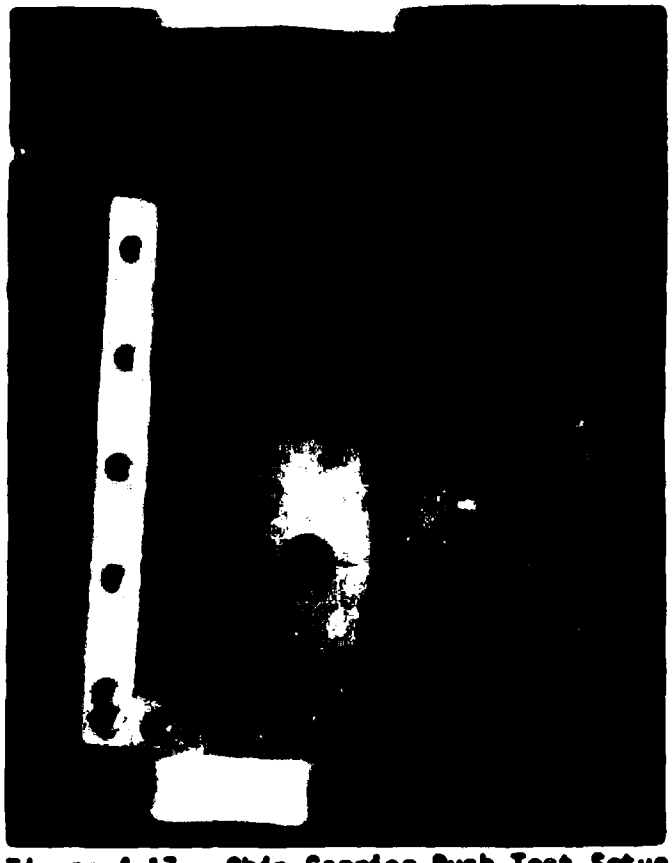


Figure 4.17 - Chip Carrier Push Test Setup.

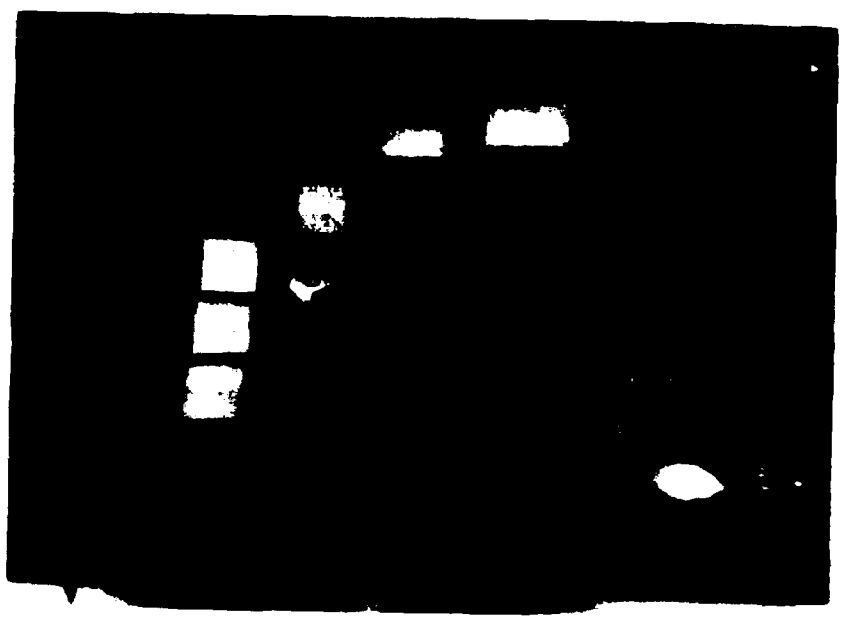


Figure 4.18 - Photograph of sample chip carrier test board after push testing. Note Teflon tape remaining under small chip carrier (center left).

Results of the temperature cycling test sequence are shown in Table 4.4 (page 67). Electrical continuity of all joints on the chip carriers was checked throughout the sequence. There were no failures or trends in electrical degradation measured.

Finite Element Modelling

The chip carrier push test was simulated using a finite element modelling (FEM) technique. Due to package symmetry, a one-eighth section of the package was used for modelling purposes, as shown in Figure 4.19. Characteristics of the chip carrier were used as inputs to the model, as shown in same figure.

The most significant difference between the model and the actual push test is in the area of applied stress. The force in actuality was applied over a circular area extending from the center of the chip carrier. Due to modelling limitations, the stress was simulated over an equal rectangular area, also centered at the center of the chip carrier. Three significant trends were shown by the model:

a) The force on each termination increases directly with the total applied force. This is shown in Table 4.5 below. An 84-termination chip carrier was modelled with total applied forces of 90, 150, and 200 pounds. In each case, the ratio of the total applied force to the highest resultant termination force was found to be nearly constant.

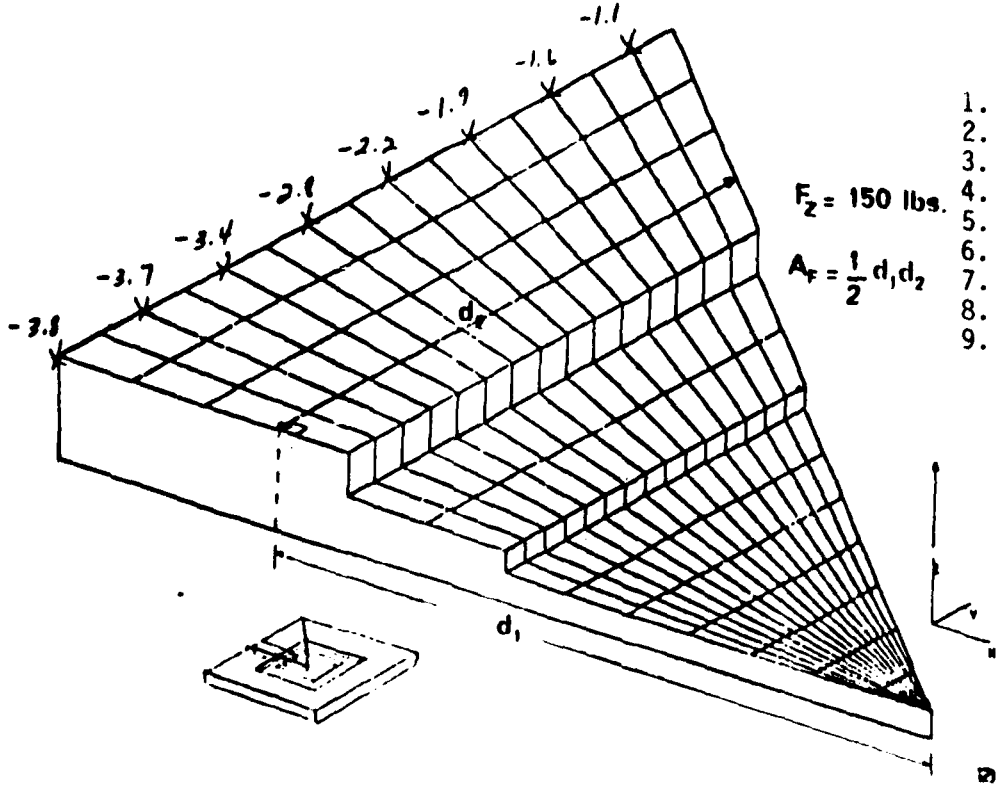
TABLE 4.5 - FEM RESULTS PREDICTING LINEAR INCREASE OF TERMINATION FORCE WITH TOTAL APPLIED FORCE

Total Applied Force (F_{Tot} - lb.)	Maximum Resultant Termination Force (F_{Res} - lb.)	Ratio F_{Tot}/F_{Res}
90	1.43	62.9
150	2.40	62.5
200	3.18	62.9

TABLE 4.4 - CHIP CARRIER PUSH TEST RESULTS
TEMPERATURE CYCLE SEQUENCE

No. of Terminations on Chip Carrier	Push Test Results (lb-force)			
	Initial	After 20 Cycles	After 40 Cycles	After 60 Cycles
20	45, 69, 77, 80, 95, 60, 75, 62, 92, 70, 60, 64	65	78	66
28	96, 78, 96, 120, 88, 78	80	76	55
44	116, 182, 192	120	116	40*
64	29, 158	66	65	109*

*Test Performed Without Tape.



Model Parameters

1. Dimensions of Package
2. Dimensions of Area Under Force
3. Location and Size of Solder Bonds
4. Package Material (Ceramic)
5. Alumina Content - 90 Percent
6. Flexural Strength - 40 kpsi
7. Young's Modulus - 50E6 psi
8. Poisson Ratio - 0.20
9. Applied Force - 150 lbs (Z)

Figure 4.19 - Finite Element Model of Chip Carrier Push Test showing model input parameters.

b) The stress concentration is greatest at the midpoints of the edges of the chip carrier, and is lowest at the corners. This is illustrated in Figure 4.20 which shows the force distribution starting from the edge midpoint, and moving to the corner for four different models (the force values have been scaled to the same edge midpoint value).

c) For solder joints of fixed size, the force on each termination decreases when both package area and number of terminations are increased. It is reasonable to assume that larger packages will utilize more terminations, both for electrical and mechanical advantages. A simulated force of 150 lb. was applied to models of: 1) a 64-termination package with a total area of 0.511 $in.^2$, and 2) a 84-termination package with a total area of 0.850 $in.^2$. The result is the graph shown in Figure 4.21. The force at each point along the package, from the mid-edge to the corner, is lower for the 84-termination package.

Conclusions

Flat Packs

There were no difficulties in performing the present test; MIL-STD-883, Method 2004, Condition B_2; on the flat packs tested in this study.

Pin Grid Arrays

The present lead integrity method did not appear to give a sufficient test of either the lead strength of our pin grid array packages (lead diameter of 0.018 in.) or the quality of the lead/package bond. The lead pull test, however, was a viable alternative.

As shown in Table 4.2, the mean pull strength was 6303 g-force with a standard deviation of 691 g-force. The three-sigma limits for the distribution would be 4230 g-force and 8376. The entire distribution of this test sample lies within these limits.

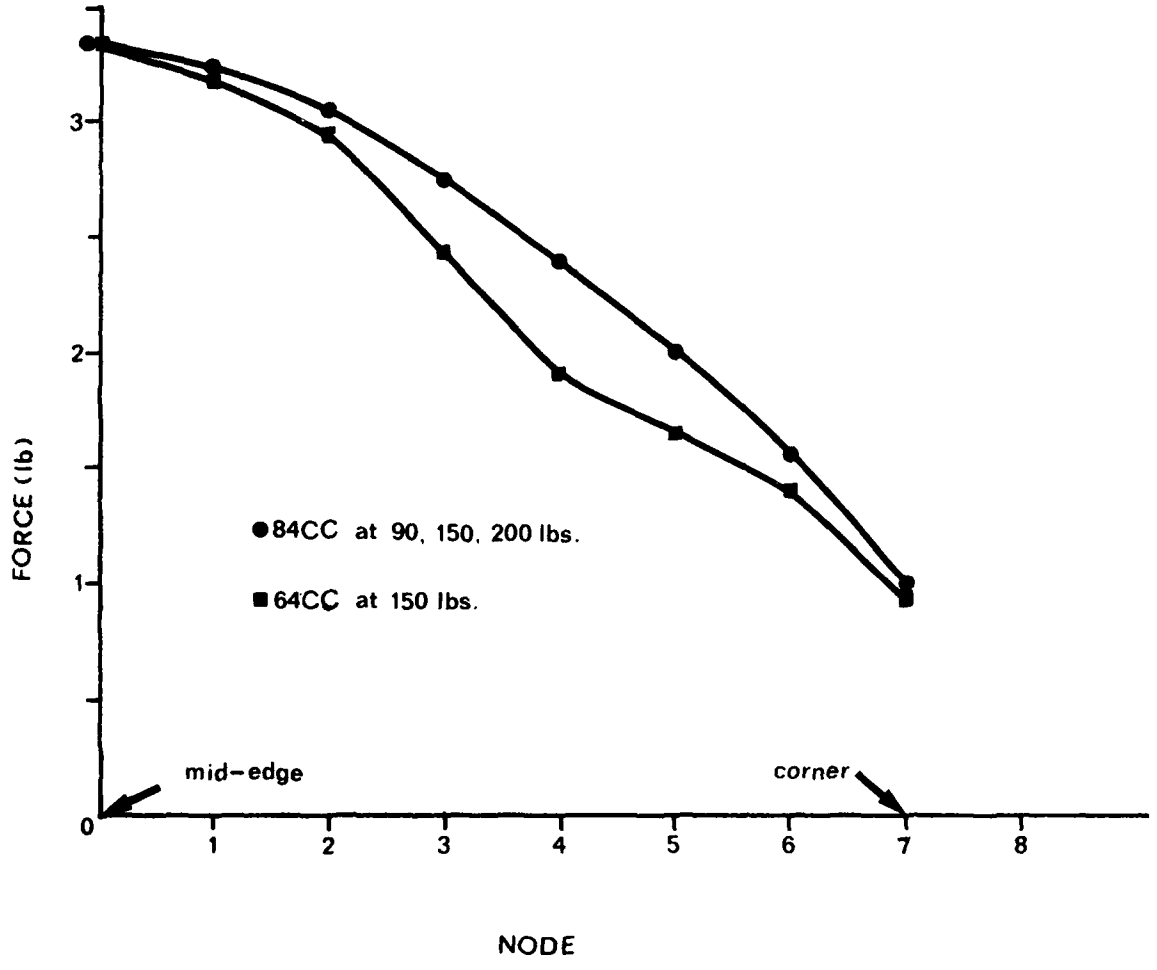


Figure 4.20 - FEM Termination Force Distribution (Scaled) Along Package Edge for Various Packages.

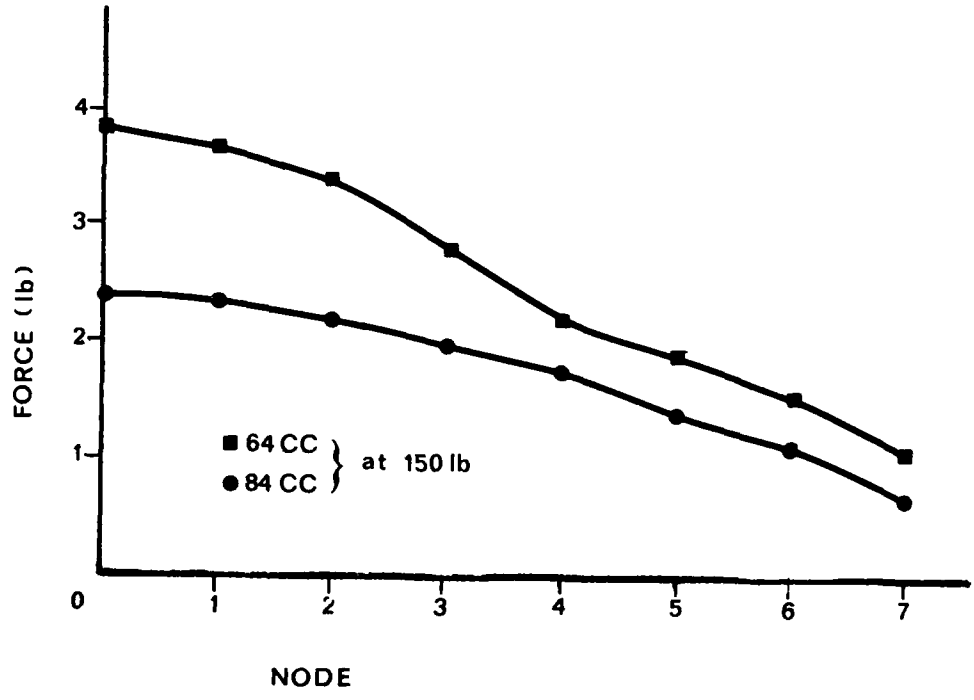


Figure 4.21 - FEM Termination Force Distribution for 64- and 84-Termination Packages Pushed with 150 lbs. total force.

The package leads for our sample had a cross-sectional area of 2.54×10^{-4} in.^{2}. This implies an average force of 2.48×10^7 grams-force per square inch of cross-sectional lead area was required for destruction. At the lower three-sigma limit, this would become 1.67×10^7 grams-force. It seems reasonable to expect all adequate pins to exceed this force rating. This becomes 1.70×10^7 grams-force per square inch of cross-sectional area as the pass/fail limit in the test method. As an example, the minimum pull strength limit of a lead with a cross-sectional area of 2.0×10^{-4} in.^{2} would be 3400 grams-force.

The new test method was written in MIL-STD-883 format and is included in the Appendix to this report. It could remain a separate method as written, or could be incorporated as a condition in the Lead Integrity Method (Method 2004).

Leadless Chip Carriers

The data used for analysis was that from the temperature cycle sequence (Table 4.4). This data was collected using the Teflon tape between the metal post and package which is the preferable test method.

For analysis purposes, certain data points from Table 4.4 were suspected as failures, and not included in statistical calculations. They were: 44-terminal package: 40 lbs. (post - 60-cycle test); 64-terminal package: 29,66, and 65 lbs.

The number of data points (N), mean value ($\overline{X}$), standard deviation (σ), $\overline{X} - 3\sigma$, and the standard deviation as a percentage of the mean ($\sigma/\overline{X} \times 100\%$) were calculated for each chip carrier type. The results were:

TABLE 4.6a - STATISTICAL ANALYSIS OF CHIP CARRIER PUSH TEST RESULTS

No. of Terminations on Chip Carrier	N	$\overline{X}$ (lb.)	σ	$\overline{X} - 3\sigma$ (lb.)	$\sigma/\overline{X}$ (x 100%)
20	15	71	13	32	18
28	9	85	18	31	21
44	6	128	55	-37	43
64	5	85	50	-63	60

The distributions for the 44- and 64-terminal chip carriers led to non-physical push strength limits and showed a large standard deviation compared to the mean. It was possible that these distributions contained failing readings and did not represent a population of normally acceptable bond strengths. To check this, the statistical parameters were calculated again (Table 4.6b) considering the 40-lb. reading of the 44-terminal package as a failure. The data for the 64-terminal devices was not used in this analysis.

TABLE 4.6b - STATISTICAL ANALYSIS OF CHIP CARRIER PUSH TEST RESULTS

No. of Terminations on Chip Carrier	N	$\overline{X}$ (lb.)	σ	$\overline{X} - 3\sigma = (X_L)$	$\sigma/\overline{X}$ x100%	$\overline{X}$ (lb.)/ Term.
20	15	71	13	32	18	3.5
28	9	85	18	31	21	3.0
44	5	145	28	30	19	3.3

For the three remaining chip carrier types, the mean push strengths per termination average out to approximately 3.3 pounds per termination. As a comparison, the Armour Research Foundation lists the tensile strength of 63Sn-37Pb solder to be near 6500 psi. Several broken solder joints were examined and the cross-sectional areas of the breaks measured to be near 0.020 in. x 0.025 in. = 0.0005 $in.^2$. The solder joint's breaking strengths can be calculated as 6500 $lb./in.^2$ x 0.0005 $in.^2$ or 3.25 lbs. That the numbers are so close is probably not as significant as the fact that they are not different by many orders of magnitude.

To this point, we are stating that on the average, the solder bonds tested withstood approximately 3.3 lbs. of tensile force before breaking. The results from finite element modelling also confirm that the total push strength should directly increase with the number of solder bonds, although a direct comparison of absolute values between the finite element model and actual measurements could not be made due to the differences in the applied force area. However, the trends observed from the modelling certainly held true for the actual test measurements.

To set a lower test limit, the values for the 20-terminal chip carrier were used because more tests were performed for that group. As shown in Table 4.6, the lowest acceptable value was chosen to be the mean of

the group minus three standard deviations. This value (X_L in the Table) was 32.1 lbs. and was 46 percent of the mean (70.5 lbs.). This figure was rounded up to 50 percent and became the standard against which the data was measured.

This standard was then generalized for all chip carrier and solder joint configurations. Using 3.3 lbs. as the mean breaking strength of the solder joints, the minimum accepted breaking strength of the joints should be 3.3 x 0.5 = 1.65 lbs. per solder joint.

From the FEM and test results, the chip carrier push strength was directly affected by the number of solder joints present. The most consistent feature of the joints is the width at the solder pad, as measured parallel to the package edge and at the package edge. This width was 0.025 in. for the solder joints of the 20-, 28-, and 44-termination chip carriers. Therefore, a minimum strength per linear inch of solder can be specified for these packages, and would be 1.65 lbs./0.025 in. = 66 lbs./in. $\sim$ 30 kg-force/in. $\sim$ 1175 g-force/mm. From this value, a minimum push strength can be calculated for any chip carrier tested by this method.

This limit was applied to the packages tested, and the results are summarized in Table 4.7. As seen in this Table, the data points originally suspected as failures (therefore withheld from limit calculations) are exactly the data points failed by the calculated minimum push strengths. Therefore, these calculated limits are self-consistent, and the 30-kg-force/in. (1175 g-force/mm) value is put forward as a reasonable lower strength limit, to be supported or modified by future data.

TABLE 4.7 - MINIMUM PUSH STRENGTHS (CALCULATED) FOR TEST PACKAGES

No. of Terminations On Chip Carrier	N	*$\bar{X}$ (lbs.)	Calculated Minimum Push Strength (1.65 lbs. x No. Terminations)	Number Passed	Number of Failures
20	15	70.5	33.0	15	0
28	9	85.2	46.2	9	0
44	6	127.7	72.6	5	1 (40 lbs.)
64	5	85.4	105.6	2	3 (29, 66, 65 lbs.)

*From Table 4.6

RECOMMENDATIONS

The following recommendations are made from the test results of Task four:

- Perform Insulation Resistance (Method 1003) as written, but do not require measurements at ±1000 V for finely spaced lead configurations, or do not use high voltage devices in finely spaced lead configurations.
- Perform Moisture Resistance (Method 1004) as written.
- Change Solderability (Method 2003) to include a new condition of 10 + 1/2 sec dwell time in the solder pot for high-mass, leadless packages.
- Allow a pre-bake condition in the Solderability Method where package plating configurations may be susceptible to aging.
- Perform Condition B_2 of Lead Integrity (Method 2004) for leaded chip carriers as written.
- Include the Lead Pull Test Method as part of MIL-STD-883, either as a separate method, or as an additional condition to Method 2004.
- Include the Chip Carrier Push Test Method as part of MIL-STD-883, either as a separate method, or as an additional condition to Method 2004.

TASK 5: DIE ATTACH EVALUATION

OBJECTIVE

To find a method to evaluate die attach quality that will be applicable to large area die.

METHOD

The evaluation approach was designed in two steps: developing test methods, and evaluating each method's effectiveness. During the effectiveness evaluation, new methods were compared with the present die shear test and also with complete etching of the die. The different methods included in the original evaluation were: radiography, infrared imaging, thermal resistance, thermal mapping, and ultrasonic imaging. These are discussed separately below. The samples were RB255 5500 gate array chips mounted into 84 termination ceramic leadless chip carriers with five different mounting materials; gold-silicon eutectic, conductive epoxy, nonconductive epoxy, gold-tin eutectic, and polyimide. Attempts to build silver-glass samples using the B255 chips and 84-termination leadless chip carriers were unsuccessful. Three silver-glass samples using 20-mil square chips mounted in ceramic dual-in-line packages were supplied by RADC for use in preliminary evaluations. However, these were not included in the step stress sequence.

Infra-Red Imaging

An infra-red microscope manufactured by Research Devices, Inc. (Model F) was used to image several of our die attach samples. Since silicon is transparent to infra-red light at wavelengths near 1100 nm, the microscope uses light of this wavelength to look through sample chips and observe the die to package bond. This is done by focusing the microscope deep into the chip and operating in a reflective mode.

The most prominent feature of the images of our samples turned out to be the surface metallization, regardless of how the microscope was focused. Aluminum of the thickness used on these samples (and typical of VLSI chips) is not transparent to infra-red light, and with the RB255 5500 gate array chips, the metallization totally dominated the image, obscuring any information that may have been gained from the die attach area.

It was then decided to end investigation of this method as it does not seem applicable to VLSI chips which have areas of very dense surface metallization.

Radiography

All of our die attach samples were x-rayed at Raytheon's Bedford Laboratories. In addition, a small number of samples were x-rayed using the Ridge Microfocus system. The Ridge system offers greater magnification, resolution, and is in general a more sophisticated system than that used at Raytheon Bedford. Both systems were adequate, however, for showing the distribution of the die attach material.

Figure 5.1 is a Ridge X-ray of a chip mounted with gold-silicon eutectic. The darker areas show the placement of the preform (intentionally small) and the spreading of the eutectic during bonding. The magnification is ∿200x and the resolution is clearly adequate for visual interpretation.

Figure 5.2 is a photograph taken from an X-ray made at Raytheon of a sample bonded with a silver-filled epoxy. Again, the location of the mounting material is clearly visible, showing inadequate coverage at the corners of the die. Note that the only information revealed is the distribution of the bonding material; no information is gained on how well that material has bonded either to the chip or to the package.

Figure 5.3 is a Raytheon X-ray of a sample mounted with a non-conductive epoxy. This material is almost completely transparent to X-rays and is not evident in this picture. Clearly, radiography will not help to assess the die attach integrity of these samples.

The X-rays of gold-tin eutectic were predictably similar in quality to those of gold-silicon, showing clearly the distribution of the eutectic. An example of this is found in Figure 5.4.

Figure 5.5 is a Raytheon X-ray of a sample mounted with a silver-filled polyimide. Again, the picture shows quite clearly the nature of the attach. Note especially the myriad voids in the attach caused by outgassing during the curing process.

In summary, radiography has proved itself to be a valid method for producing a clear image of the die attach region of samples mounted with gold-silicon eutectic, conductive epoxy, gold-tin eutectic, and polyimide. Non-conductive epoxy does not lend itself to the radiographic technique, however.

It should be emphasized that, for all X rays, only the presence of the bonding material is assured. Non-wetting and dewetting of the material will not be detected by this method. Therefore, a sample with an X-ray showing total coverage of the area under the die by the bonding material may in fact be nearly completely unbonded. It is for this reason that X-ray alone cannot sufficiently evaluate die attach integrity.

Figure 5.1 - Ridge X-ray of die bonded with gold/silicon eutectic. Note: large rectangular dark area is preform.

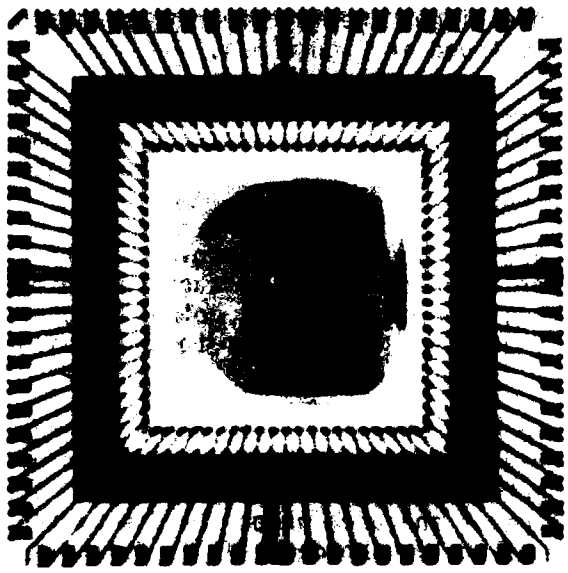


Figure 5.2 - Raytheon X-ray of die bonded with silver-filled epoxy. Note absence of epoxy under upper and lower left corners of die.

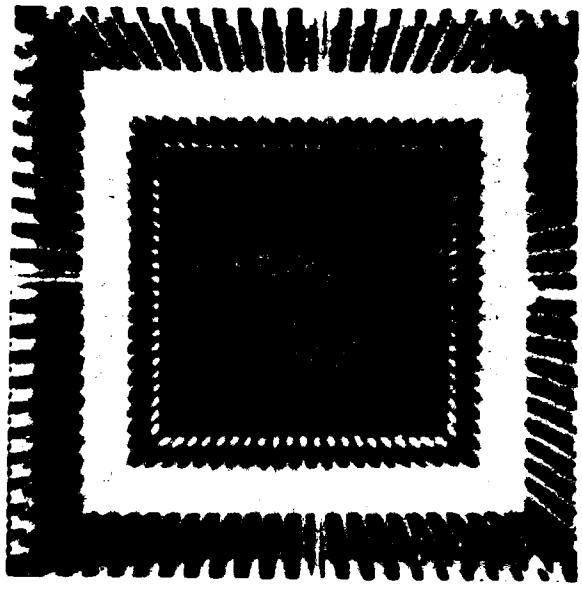


Figure 5.3 - Negative X-ray image of sample bonded with non-conductive epoxy. Central dark die bond area indicates that the epoxy is invisible to X rays.

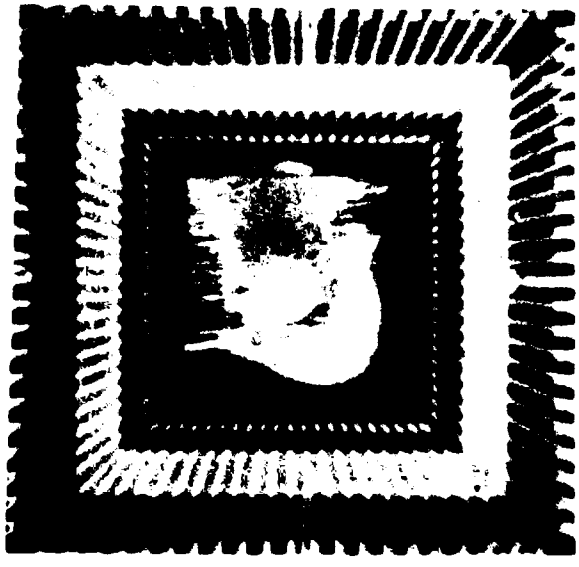


Figure 5.4 - Negative X-ray image of sample bonded with gold/tin eutectic. Lighter areas under die indicate presence of eutectic. Again, coverage under the die is not complete.

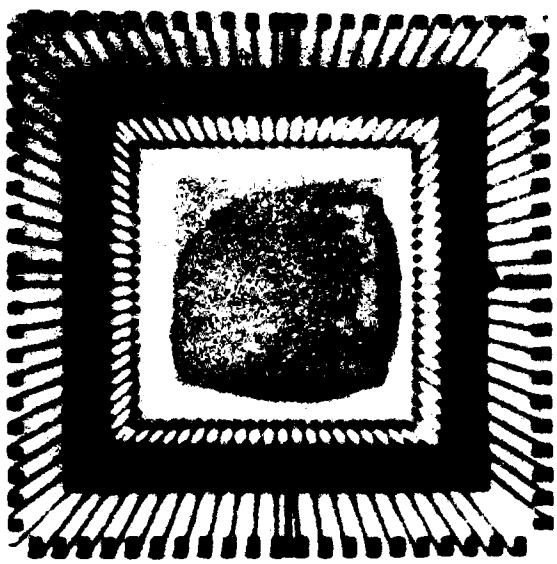


Figure 5.5 - Positive X-ray image of sample mounted with polyimide. Note myriad voids typically produced by outgassing during the curing process.

Thermal Resistance

Thermal resistance measures the temperature rise in a semiconductor device as a function of the applied power. The temperature rise can be referenced to the case temperature (Θ_{jc}) or the ambient temperature (Θ_{ja}). Since the temperature rise with applied power depends on how much heat energy a particular device can conduct, thermal resistance is also a measure of the thermal transfer properties of the device. Thermal transfer depends on the geometry and materials in the heat conduction path which, in the case of an integrated circuit chip, includes the die attach. Thus, thermal resistance can be used as an indication of die attach quality.

Adapting thermal resistance tests to measure the die attach quality of a large VLSI/VHSIC chip required two modifications in the normal test method. To include as much of the die attach area as possible, eight pin locations were chosen for thermal resistance measurements on each sample. These eight pins were selected to provide measurements of Θ_{jc} and Θ_{ja} on each of the four sides of the chip.

Another problem was the low power dissipation of the CMOS bulk devices on the test samples, two RB255 5500 gate arrays. With V_{DD} applied, only 25 mW of power was dissipated. To perform these tests at 25 MHz under dynamic operation required prohibitively expensive and time consuming design and construction of exercising circuitry. An alternate method was developed which essentially "reverse biased" the input/output structure under test. Ground was made positive and the selected package pin was grounded. In this way, power dissipation was increased to 130 mW in each thermal resistance path tested.

The test circuit used to make the thermal resistance measurements is shown in Figure 5.6. The circuit is used to measure the voltage in the path when the particular input/output was powered to 130 mW and when only a steady state current of 250 μamp was flowing. This voltage difference could be converted to a temperature value using measurements of the path's thermal characteristic (mV/°C). The junction temperature is this temperature value added to the ambient temperature. Calculation of Θjc is performed by taking the difference between junction and case temperature divided by the applied power. The value Θja is the difference between the junction and ambient temperature divided by the applied power.

Table 5.1 summarizes the thermal resistance measurements on the two gate arrays. All values are listed in °C/W. The last two columns represent the difference between initial readings on one device and repeated measurements of the same device.

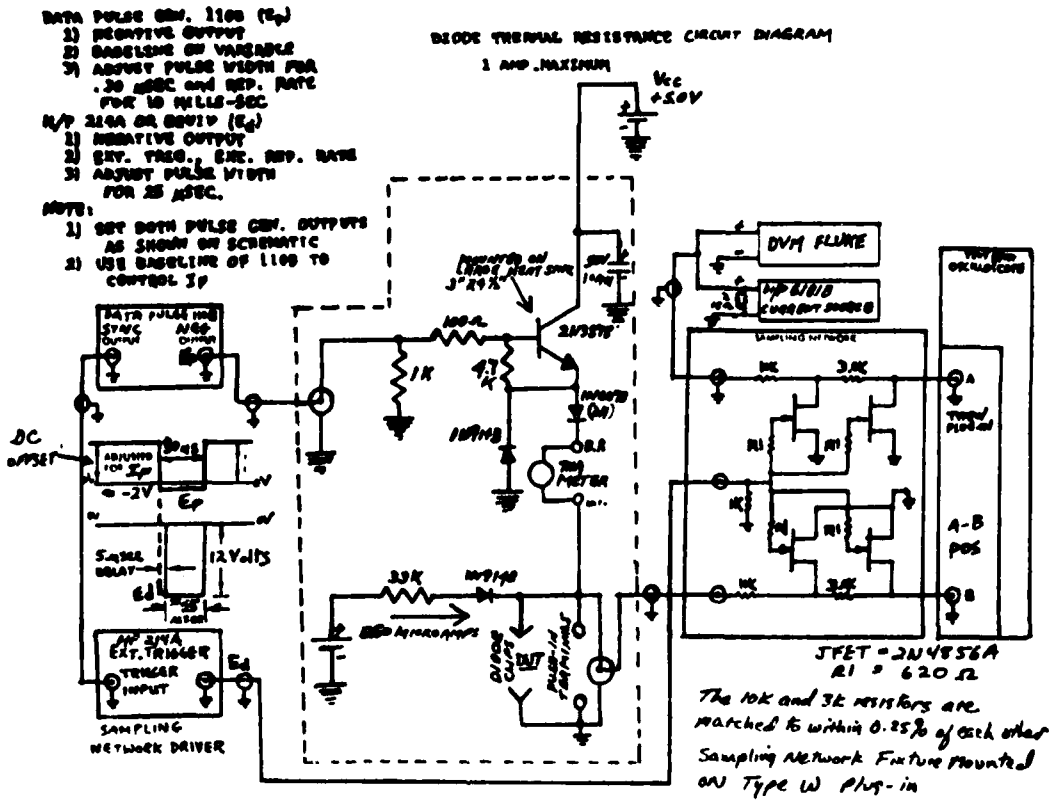


Figure 5.6 - Test circuit used to make thermal resistance measurements.

TABLE 5.1 - THERMAL RESISTANCE SUMMARY

Pin Number to +GND	S/N 370 Initial		S/N 371 Initial		S/N 371 Repeat		S/N 371 Initial Versus Repeat	
	Θjc	Θja	Θjc	Θja	Θjc	Θja	Θjc	Θja
47	8.45	71.5	--	--	--	--	--	--
14	17.93	81.28	14.35	80.46	11.58	75.11	2.77	5.35
73	9.13	70.5	6.26	77.54	8.72	66.62	2.46	10.92
26	14.41	71.1	12.24	78.04	10.31	74.98	1.93	3.06
51	15.5	75.2	16.55	68.52	8.653	72.82	7.9	4.3
61	15.33	73.23	9.74	77.4	8.246	79.56	1.49	2.16
68	14.61	74.73	14.9	79.39	13.51	78.49	1.39	0.9
82	14.28	74.96	13.49	79.44	12.69	81.9	0.8	2.46
30	--	--	6.02	72.09	6.32	68.82	0.3	3.27

NOTE: Pin 47 Circuit not acceptable on S/N 371

Pin 30 Circuit not acceptable on S/N 370

From the figures in the last two columns, note that the average change in Θjc readings was 2.38°C/W and in Θja readings 4.05 °C/W. Referencing to the initial reading shows relative errors ranging from a high of 48 percent (7.9/16.55) to a low of 1 percent (0.9/79.39). In relative error, Θja was more repeatable in general with an average of 5 percent where Θjc had an average relative error of 20 percent. It seems realistic to treat the values for Θjc as varying by about 20 percent and for Θja by 5 percent.

The only 20% variation in the θjc readings for S/N 370 was the difference between pins 47 and 73, and the remaining test pins. In θja readings, pin 14 alone differed by greater than 5% from the remaining pins. For S/N 371 θjc readings, pins 73 and 30 differ the most from the remaining pins, and pin 61 shows some difference from the other device pins. In θja readings, pins 51 and 30 differ from the remaining pins.

To determine the possible source of these different readings, both the chip surface and the die attach were investigated. The RB255 chip has two different input/output structures as shown in Figure 5.7(a) and (b). Figure 5.7(a) is of pin 14 which was similar in structure to pins 26, 51, 61, 68, and 82. Figure 5.7(b) shows pin 30 which was similar to pins 47 and 73. This variation in I/O structure accounts for the differences in S/N 370 θjc readings and the pin 30 and 73 difference in S/N 371 θjc. These were the quantitatively largest significant variations observed in the data.

X-rays of the die attach areas of the two devices are shown in Figure 5.8. On S/N 370, voids are apparent near pins 14, 26 and 82. This voiding is not reflected in the measurements of θjc (17.93, 14.41, and 14.28 °C/W respectively) or in θja (81.28, 71.10, 74.96 °C/W respectively) although the θja pin 14 value is somewhat larger than the other θja values. On S/N 371, voids are most noticeable near pins 14 and 82. There is also some voiding in the pin 36 and 30 region. The θjc values for pins 14 and 82 (14.35 and 13.49 °C/W) and for 26 and 30 (12.24 and 6.02 °C/W) did not show any trend related to these voids. The θja values for the four pins (80.46, 79.44, 78.04, and 72.09) did not reflect the presence of voids either.

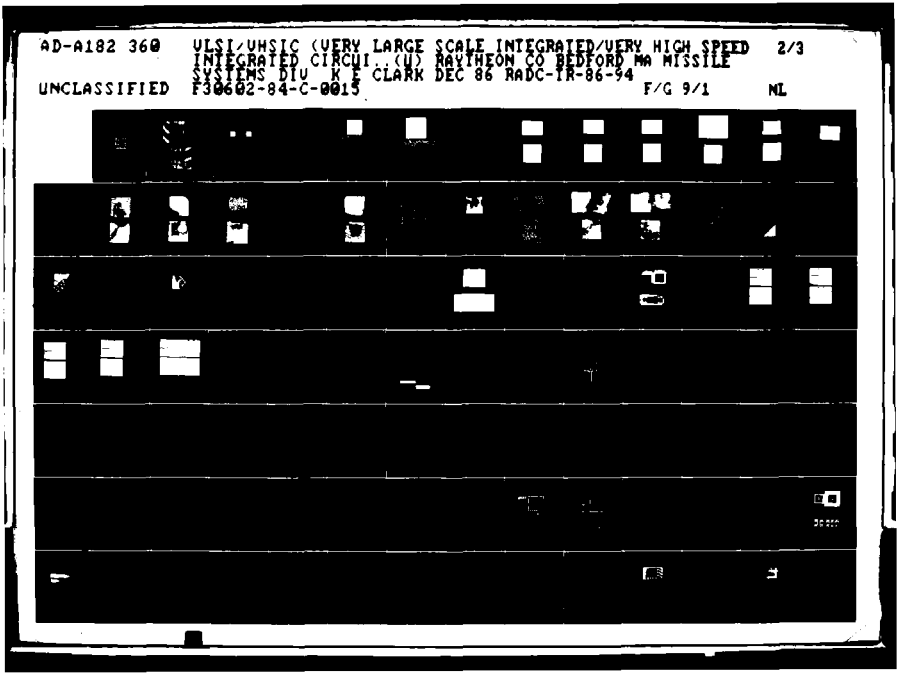
The conclusion is that thermal resistance values vary more with the electrical structure of the test path than with die attach integrity. Thus, thermal resistance was eliminated as a possible approach for further test method development.

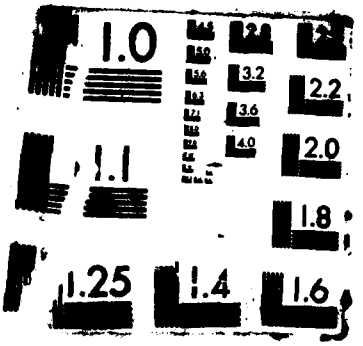
Thermal Mapping

The premise behind thermal mapping is to use the thermal transient properties of the die attach material to gain information about its existence and adhesion beneath the die. To this end, sample packages were [illegible] on a uniformly heated stage and the top of the chip imaged (by several systems) to detect the distribution of heat reaching the surface of the chip through the die attach interface. Thus, a cool spot on the chip surface corresponds to a void directly beneath that area in the die attach material.

Three IR imaging systems were used on our samples: the [illegible] a system manufactured by Hughes, and Barnes Engineering's [illegible] these, the UTI and Barnes systems were examined closely [illegible]

AD-A182 360 VLSI/VHSIC (VERY LARGE SCALE INTEGRATED/VERY HIGH SPEED 2/3
INTEGRATED CIRCUI..(U) RAYTHEON CO BEDFORD MA MISSILE
SYSTEMS DIV K F CLARK DEC 86 RADC-TR-86-94
UNCLASSIFIED F30602-84-C-0015 F/G 9/1 NL

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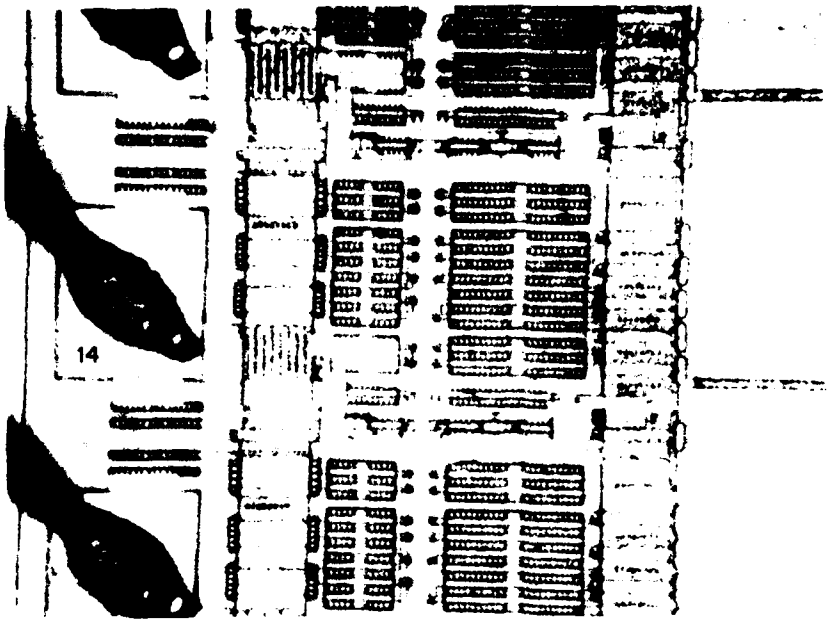


Figure 5.7(a) - Pin 14 on RB 255. This structure identical to pins 26, 51 61, 68, and 82.

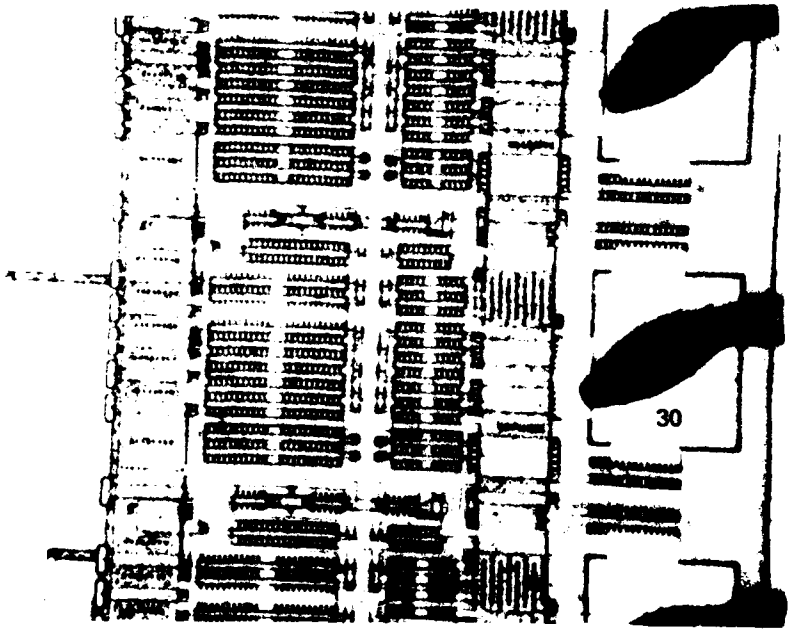


Figure 5.7(b) - Pin 30 on RB 255. This structure identical to pins 47 and 73.

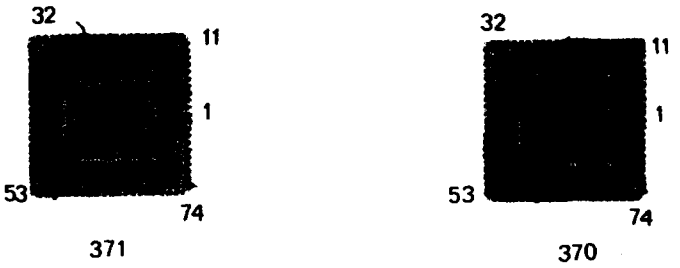


Figure 5.8 - X-rays of die attach area on RB 255 thermal resistance samples. The numbers around the package periphery are the package pin numbers at that point. The serial numbers are below each image.

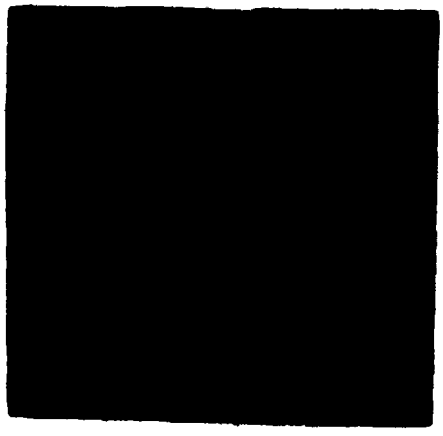
more suited to imaging large components than imaging microelectronic devices, and no images were recorded using this system. The results from the other two systems follow.

The UTI system used did not offer the spatial resolution necessary to sufficiently image the chip surface. Figure 5.9 is a thermal image of a chip bonded with non-conductive epoxy. Red and white pixels represent the warmest regions (45°C), and black and violet the coolest (43°C). The thermal resolution used for the image is 0.1°C per color level. The image is updated every 1.5 sec, and for our samples, no two frames ever appeared similar, probably due to the working distance between sample and detector (about 5 ft.). A 2.5X image enlarger attachment was available, but using this attachment distorted the image, as the detector then tends to image itself - a factor which cannot be eliminated (according to the manufacturer). Attempts were made to decrease the working distance, but it could not be shortened enough to prevent the airflow between the sample and detector from causing a constantly varying image of the chip's surface temperature.

In view of the inadequate resolution and instability of the thermal images generated by the UTI 9000, consideration of this system for die attach evaluation was abandoned.

In contrast, the Barnes Engineering CompuTherm, using a calibrated heated substage and microscopic objective detector, reduced the working distanceto a fraction of an inch thus providing a high-resolution stable thermal image of the samples tested.

The primary difficulty encountered in trying to produce a temperature map of a chip surface is eliminating the effects of surface variations in emissivity (a material characteristic) and topology. The CompuTherm is equipped with software which can calculate the emissivity of a sample on a point-by-point basis, and then correct the image displayed for the various emissivities of the sample. Figure 5.10 is a photograph from the CompuTherm's video screen displaying such an image of approximately one quarter of a sample chip. Two things are apparent from the picture: the first is that there are distinct variations in the heat reaching different locations of the chip surface. The lower half of the chip image shows variations in surface heat which do somewhat correspond to locations of the die attach material (as determined from X rays). What appears equally clear, however, is that the image details stem mainly from the configuration of the surface materials. The large blue rectangular region of the figure is an area of dense aluminum metallization (the gate region of the chip), showing that it actually is cooler than the surrounding regions.



MAG ~ 4.5X

Figure 5.9 - Thermal image of chip surface generated by UTI 9000. Chip measures 350 x 350 mil. White indicates warmest areas (44.6°C), violet indicates coolest (43.1°C).

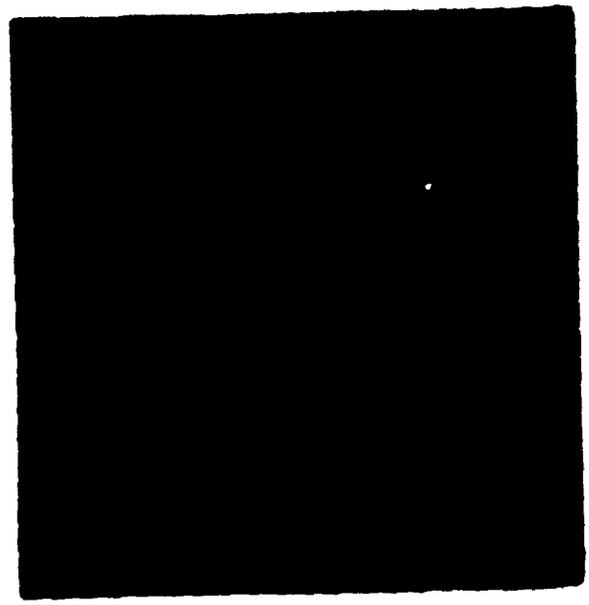


Figure 5.10 - Thermal image of ~ 1/4 of sample chip surface as produced by Barnes Engineering's CompuTherm (photographed) from video monitor. Sample was heated from underneath. Lower half of image shows differences in surface heat from die bond variations. Upper half shows surface heat differences due only to surface topology (i.e., large blue area is dense gate metallization).

Even when the image is corrected for emissivity, the fact remains that surface characteristics cannot be eliminated from thermal images produced in this way. The thermal surface variations produced by die bond characteristics cannot be isolated with confidence. This is not a reflection of the quality of the test equipment (which is excellent), but of the utility of the test method attempted. For this reason, no further investigation of thermal mapping as a test method for die attach evaluation will be conducted.

Ultrasonic Imaging

Ultrasonic imaging as applied to microelectronic devices is a relatively new technique although the original concept dates back to 1936. This method was not part of the original proposal, but was included for further investigation when it became apparent that the technique was applicable to die attach evaluation. The performance of equipment manufactured by three vendors was evaluated: Sonoscan, Inc.; Panametrics, Inc.; and J. B. Engineering. In each case the basic principle was the same: an image was made of the sound transmission through the sample.

The equipment manufactured by J. B. Engineering was designed for large castings and could not be readily adapted to our samples.

Sonoscan, Inc., used a scanning laser acoustic microscope (SLAM) to perform the imaging. A sample was placed on a piezoelectric crystal transducer capable of producing sound waves at 10, 30 or 100 MHz. A gold foil cover slip was placed over the sample, in physical contact with the die surface. The sample, cover slip and transducer were immersed in distilled water to eliminate air gaps. In operation, the foil had wrinkled or flat areas corresponding to areas of the sample that conducted or didn't conduct sound waves.

An image of these patterns on the gold film was formed with a scanning helium-neon laser. The reflection angle of the laser beam was translated into an optical intensity pattern which showed where wrinkles or flat areas of the foil occurred. This image was displayed on a cathode-ray tube screen.

Five samples of each die attach material and an additional three silver-glass samples were imaged using Sonoscan's SLAM. The gold/silicon and gold/tin eutectic samples had clear images that correlated well with X-ray images. Both X-ray and SLAM images showed the presence of epoxies, but the SLAM images showed more details in the bonded regions. The opposite was true of polyimide samples which showed greater detail in X-rays than the SLAM images. The X-ray images of non-conductive epoxy samples were entirely featureless while SLAM images showed varying degrees of bonding. Silver-glass samples were uniform in appearance in both X-ray and SLAM images. Examples are shown in Figures 5.11 - 5.16.

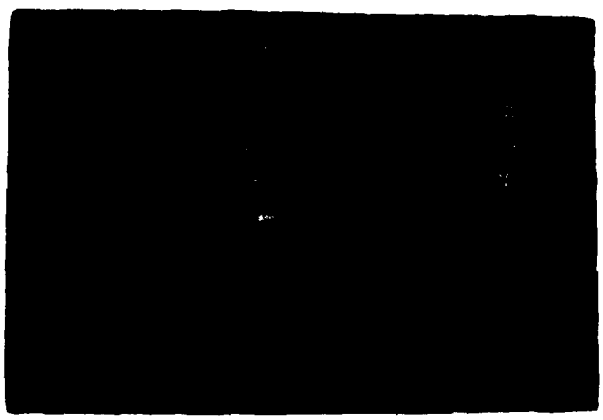


Figure 5.11(a) - SLAM image of die bonded with gold/silicon eutectic. Lighter areas show bonding.

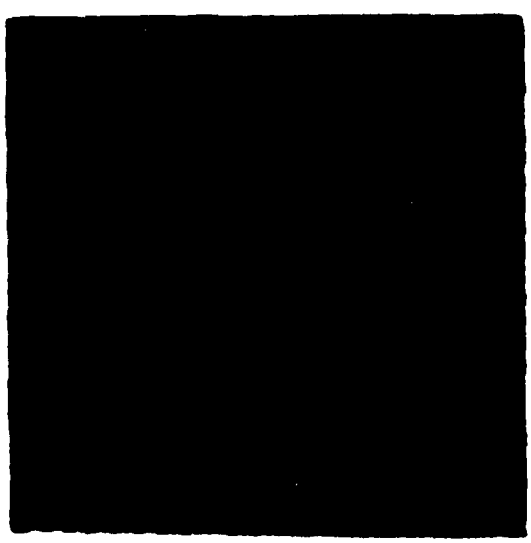


Figure 5.11(b) - X ray image of above sample.

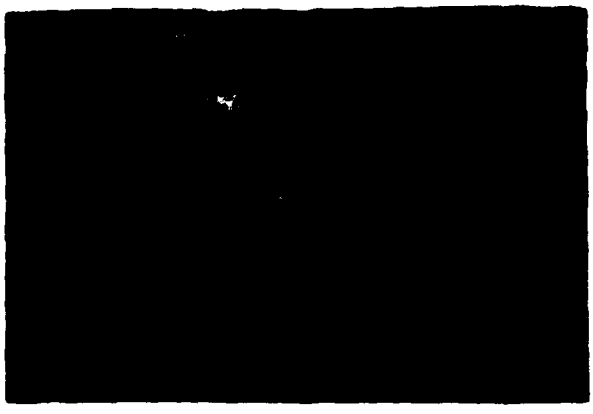


Figure 5.12(a)- SLAM image of die bonded with silver-filled epoxy.

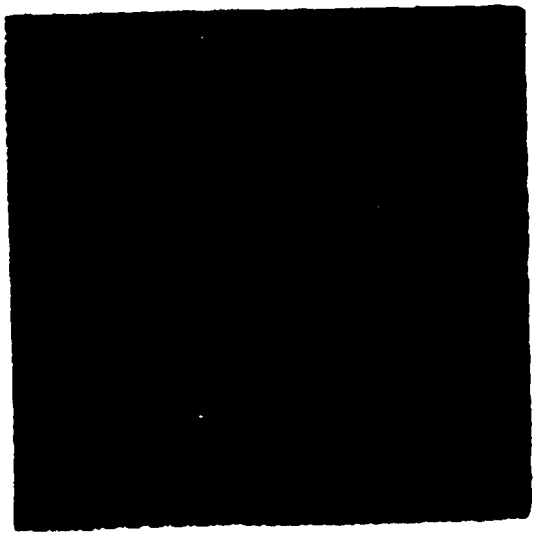


Figure 5.12(b)- X ray image of above sample.

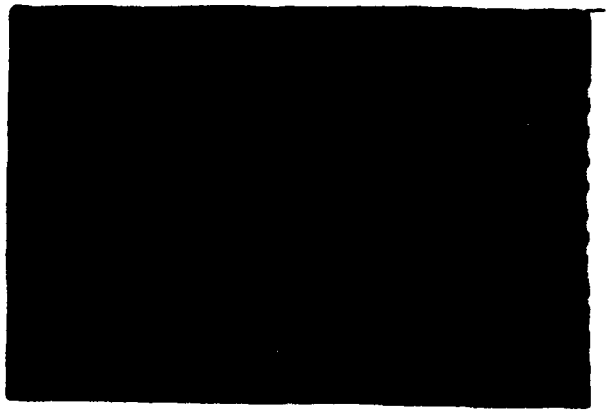


Figure 5.13(a) - SLAM image of die bonded with non-conductive epoxy.

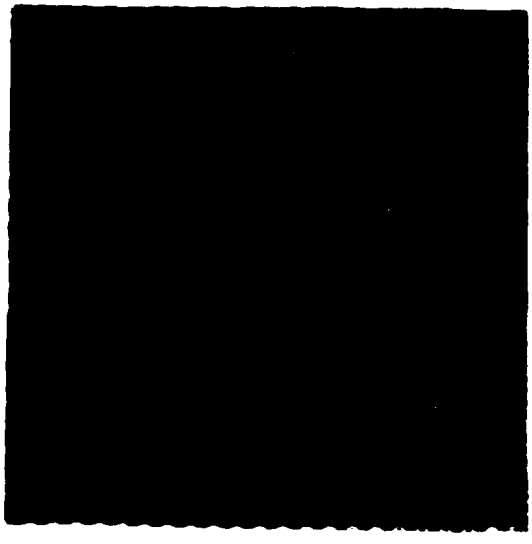


Figure 5.13(b) - X ray image of above sample.

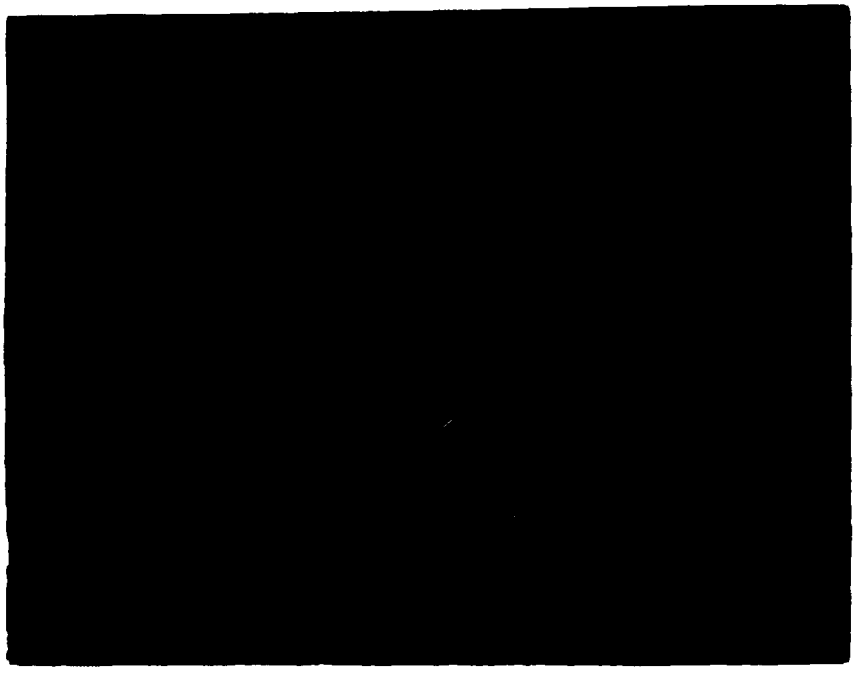


Figure 5.14(a) - SLAM image of die bonded with gold/tin eutectic.

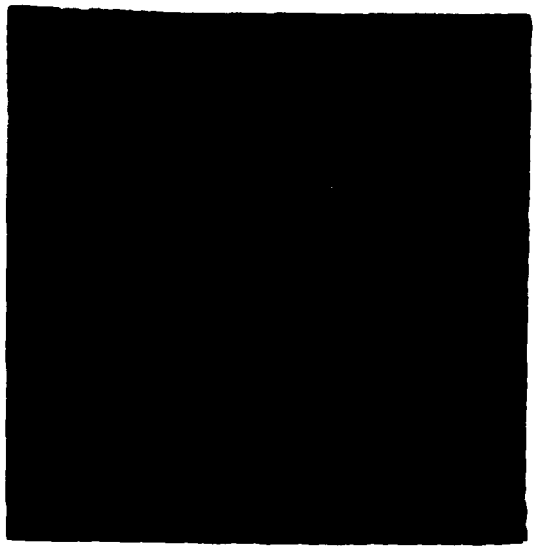


Figure 5.14(b) - X ray image of above sample.

Figure 5.15(a) - SLAM image of die bonded with polyimide.

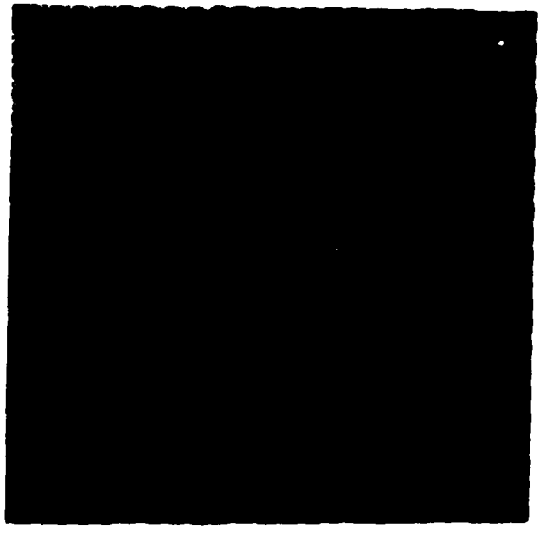


Figure 5.15(b) - X ray image of above sample.

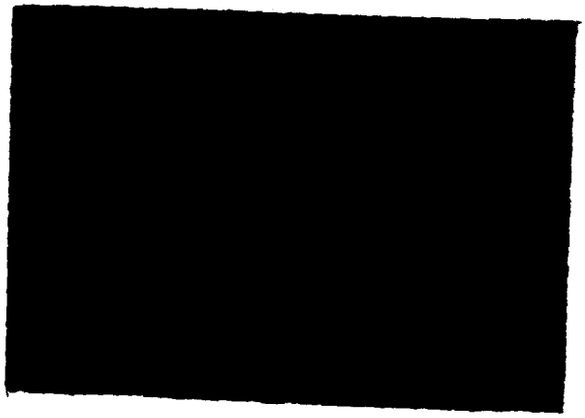


Figure 5.16 - SLAM image of die bonded with silver-glass.

Although the SLAM images of the die attach areas were promising, the samples could only be imaged while delidded and immersed in fluid. This may not be practical for all devices that might use the test method, thus,an alternate system manufactured by Panametrics that could image through the back of a sealed package was also investigated.

Panametrics used the Hyscan Model I system to image the die attach samples. The Hyscan impinges the sample under test with an ultra-high frequency (50 - 100 MHz) acoustic wave, detecting the reflected signal from the sample. The depth of the reflecting layer was selected electronically; signals from this depth level were then quantized into a sixteen-level grey-scale for printing. The output was a hard-copy C-scan image.

Samples had to be immersed in a liquid to provide acoustic continuity between the transducer and sample. The reflected signal could be recorded from either the die surface or the back of the package. Although the samples used here were unsealed, the reflection signal from the back of the package would be the same as that from a sealed package.

Five samples were imaged using the Hyscan system. Both gold/silicon and gold/tin eutectic samples showed close correspondence with X-ray images, and greater detail than the Sonoscan system. The conductive epoxy ultrasonic image was more detailed then the X-ray image, and the non-conductive epoxy ultrasonic image showed structure where none was apparent from the X-ray. Unlike the Sonoscan system, the Hyscan images were comparable to X-ray for the polyimide sample. The gold/silicon eutectic sample was also imaged from the back of the package. This image was poorer in quality than the original frontal image, but was superior to the Sonoscan image. See Figures 5.17 to 5.22 for comparison.

Using ultrasonics for evaluating die attach integrity appeared to be very promising. For our samples mounted with gold/silicon eutectic, gold/tin eutectic, conductive epoxy, and polyimide, ultrasonic images closely (if not perfectly) corresponded to X-rays of the same samples, and in the case of Panametrics, with excellent resolution. This was also the only method explored which would image (to any degree) a non-conductive epoxy die attach sample, although with less clarity than it imaged samples with other bonding materials. Even when apparently similar to X-rays, ultrasonic images are images of where the bonding material wets bonded surfaces (die and substrate), not merely images of where the bonding material is located under the die.

Of the two systems investigated, Panametrics offered better resolution, depth selection (the interface to be imaged is directly selectable), and magnification capabilities for imaging microelectronic devices. Also, in cases where the ultrasonic wave itself will not damage a device, the Panametrics system did not require delidding of hermetically sealed samples for imaging, thus providing a non-destructive test. The die attach

Figure 5.17 - Hyscan C-scan of chip attached with gold/silicon eutectic.

Figure 5.18 - Hyscan C-scan of chip attached with conductive epoxy.

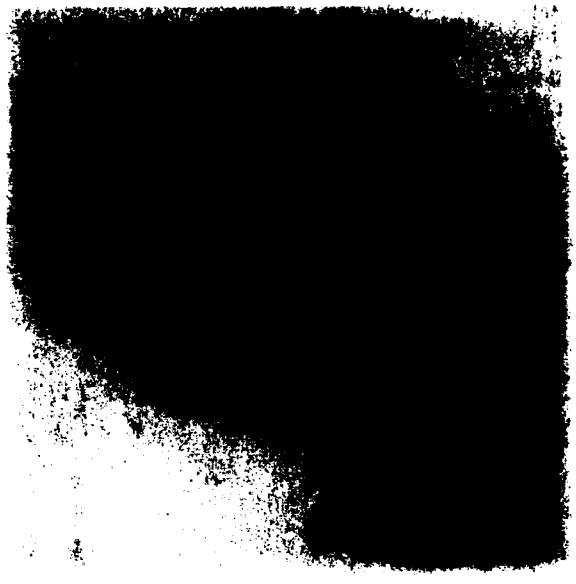


Figure 5.19 - Hyscan C-scan of chip attached with non-conductive epoxy.

Figure 5.20 - Hyscan C-scan of chip attached with gold/tin eutectic.

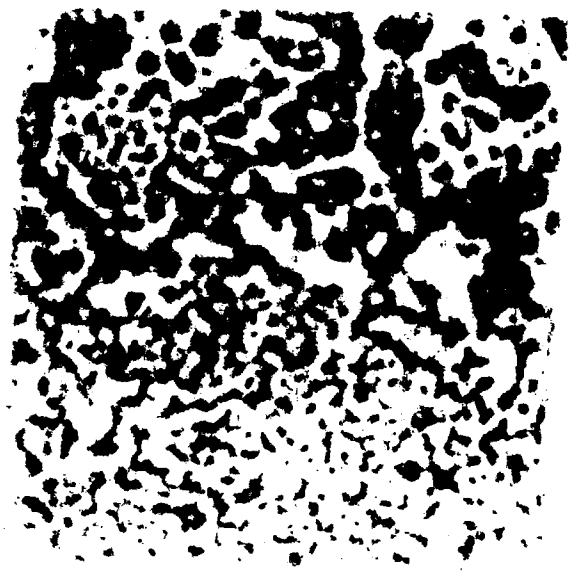


Figure 5.21 - Hyscan C-scan of chip attached with polyimide.

Figure 5.22 - Hyscan C-scan made from the back of the package of the sample shown in Figure 5.18.

interface could be accessed through the substrate and the signal reflected back to the detector. Sonoscan's SLAM, however, requires transmission of the signal through the sample, therefore,the air gap between die and lid must be eliminated if an image is to be produced.

The die were etched from selected samples to reveal the bonding material. One such sample and its initial ultrasonic image are shown below as Figure 5.23(a) and (b). The patterns correlated well with both X-rays and ultrasonic images.

Two methods were chosen for further evaluation: X-ray imaging and ultrasonic imaging. These methods were then compared through an environmental stress sequence. The test plan for this effort is described below.

ENVIRONMENTAL TEST SEQUENCE

Method

Fifty samples were constructed for the die attach evaluation. For all samples, RR255 chips (0.350 in. x 0.350 in.) were mounted into 84-termination ceramic leadless chip carriers with an outer dimension of 0.922 in. x 0.922 in. The samples were divided into five groups of ten samples each, and each group was assembled with one of the following five different bonding materials: gold-silicon eutectic, conductive epoxy, non-conductive epoxy, gold/tin eutectic, and polyimide. Three samples of each bonding material were to be subjected to each environmental stress test, with one sample of each bonding material held as a control. The samples then were subjected to the test plan shown in Figure 5.24.

The initial, interim, and final tests performed were visual inspection, radiography, and ultrasonic imaging. All of the above tests were performed following each environmental stress level. In addition, five samples (one of each mounting material) were die sheared in accordance with MIL-STD-883, Method 2019. The die shear test was totally ineffective in evaluating the die bond integrity. A typical result is shown as Figure 5.25. In each case, the die fractured at the location of stress application, and at a force much greater than the minimum 2.5 kg-force. As a result, efforts in this direction were discontinued.

Results

The test plan was completed with only two samples failed during the entire environmental stress sequence. Both were bonded with gold/tin eutectic, and both failed due to chip fracture and partial lift-off during constant acceleration at 30,000 g.

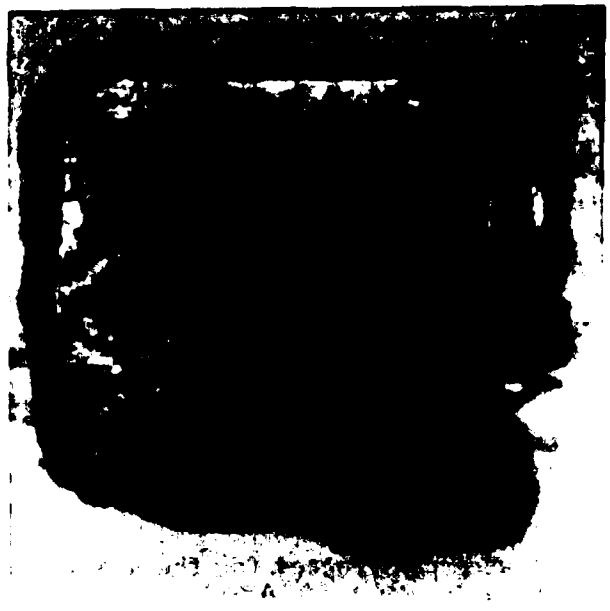


Figure 5.23(a) - Sample with die partially etched reveals distinctive bonding pattern at left.

Figure 5.23(b) - Ultrasonic image of above sample reveals the same pattern.

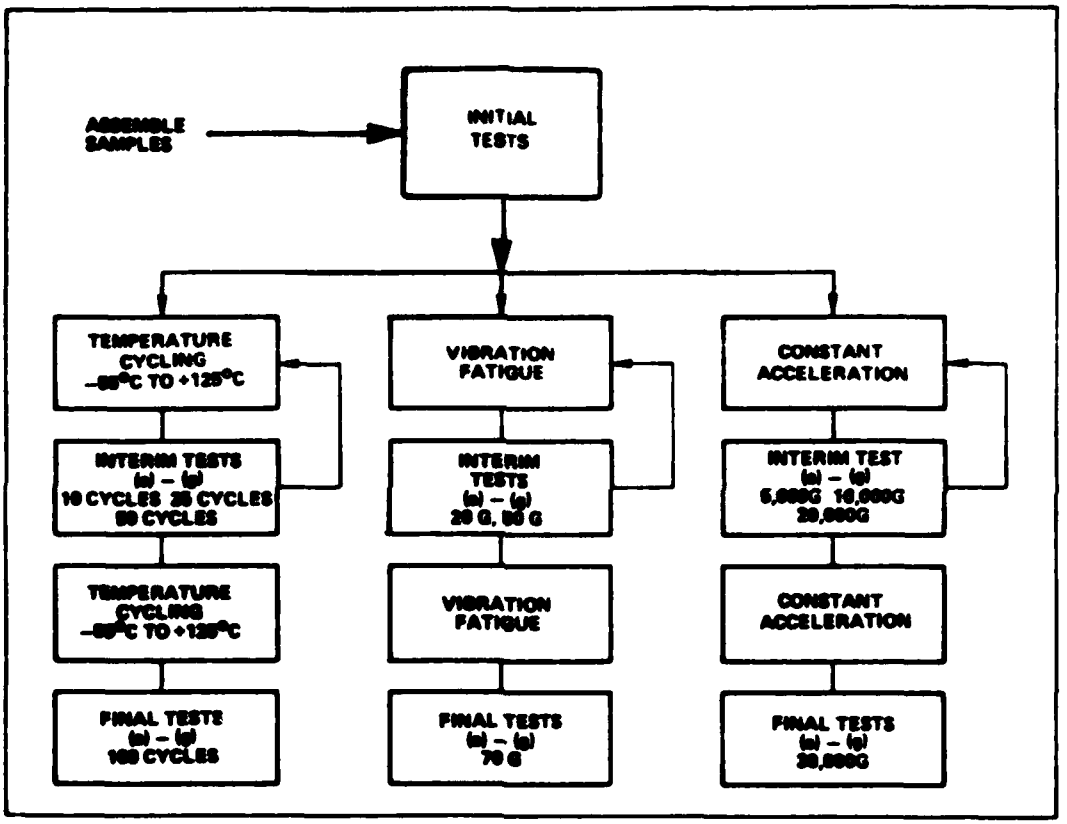


Figure 5.24 - Die Attach Evaluation environmental test plan.

Figure 5.25 - Die fracture as a result of die shear strength testing.

Figure 5.26 shows the first failed sample beside its corresponding initial X-ray and initial ultrasonic image. The darker areas of the X-ray indicate the presence of eutectic material under the die, while the lighter areas of the ultrasonic images indicate areas where the eutectic present is actually well bonded to the chip. It can be seen that the X-ray shows the presence of eutectic in the corner of the die which lifted off, while the ultrasonic image (taken through the die) shows no bonding in that region. The same is true for the second failed sample, shown in Figure 5.27. From these two figures, it can be concluded that the ultrasonic images accurately reflect the degree of bonding in the samples. This is information that X-rays do not provide.

The X-rays and ultrasonic images of the samples also reflect the low failure rate of samples during the environmental test sequence. A comparison of initial to final X-rays and initial to final ultrasonic images reveals that in both cases the recorded image did not appreciably change for any sample as a result of the stress sequence.

The initial and final ultrasonic images for all samples were then analyzed to determine which features of the images would predict poorer performance from the two samples which actually failed.

The degree of bonding of each sample was determined in the following manner: A 10 x 10 grid was first superimposed over each image. This was done by drawing the grid on a transparent sheet of acetate and then placing the sheet over the image. Each square in the grid was examined for bond area. The square was counted as being bonded if it was at least 50 percent bonded, and counted as unbonded if less than 50 percent bonded. Since the image was divided into 100 equal squares, the total number of the "bonded" squares equalled the total percentage of die bonding for the sample. A frequency distribution of bonding percentage for all samples is shown in Figure 5.28. As can be seen from the histogram, the majority of the samples were more than 50 percent bonded.

The MIL-STD-883 test method for radiography (Method 2012) provides criteria for analyzing radiographic images of the die attach. The failure criteria stated in that method are: 1) the bonding material must be present over at least 50 percent of the intended contact area, and 2) the sample fails if any single void extends from one edge to its opposing edge and covers more than 10 percent of the total intended contact area. Figure 5.29 illustrates these criteria (Figure 2012-1 from the test method). Figure 5.30 shows an example of a bonding material distribution which would pass the radiographic failure criteria. The area under the die is more than 50 percent covered with bonding material, and the voided area, while covering much more than 10 percent of the total intended contact area, does not extend completely across either the length or width of the die. Obviously, this is not a

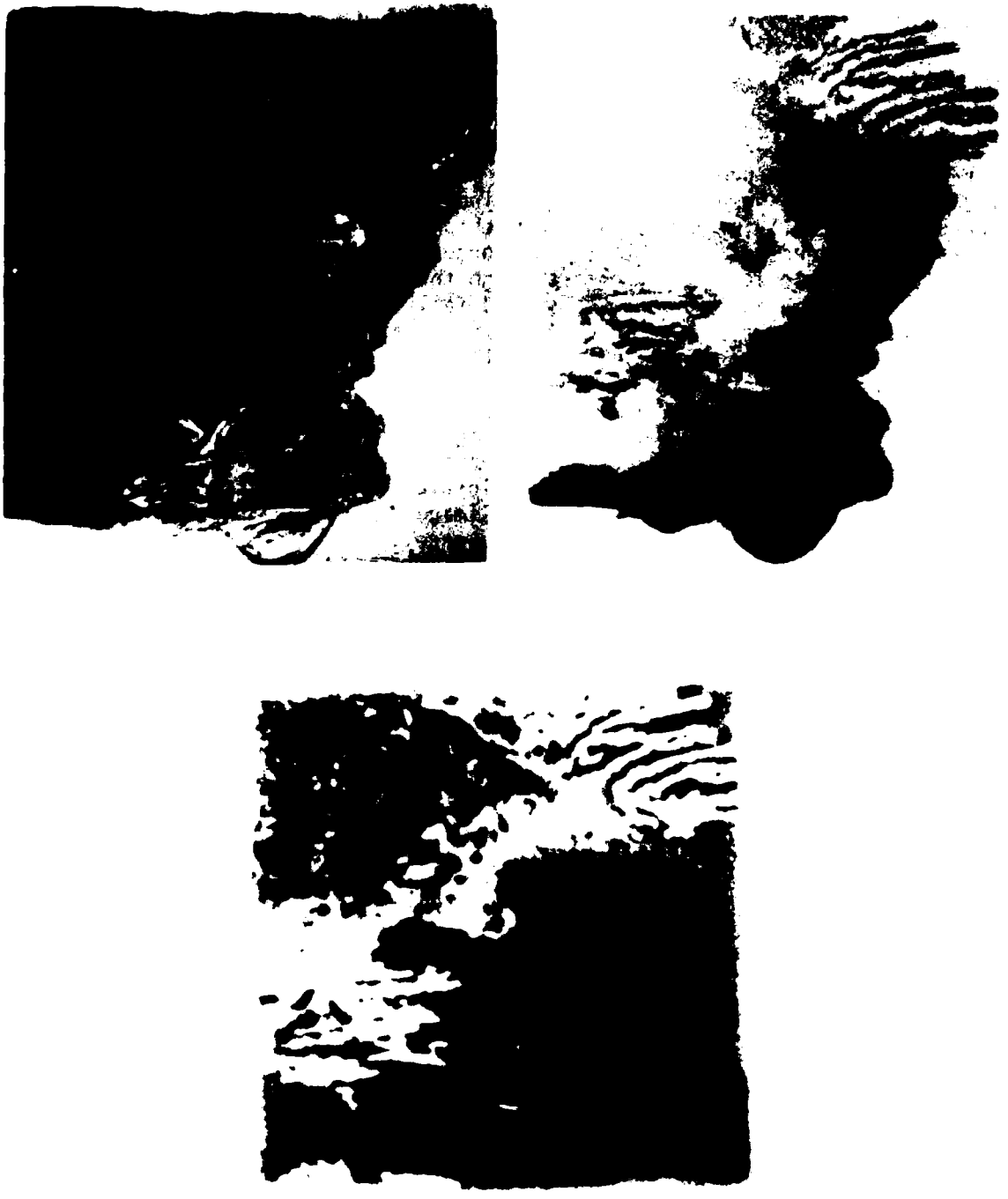


Figure 5.26 - Optical photo, X-ray, and ultrasonic image of failed device.

Figure 5.27 - Optical photo, X-ray, and ultrasonic image of second failed device.

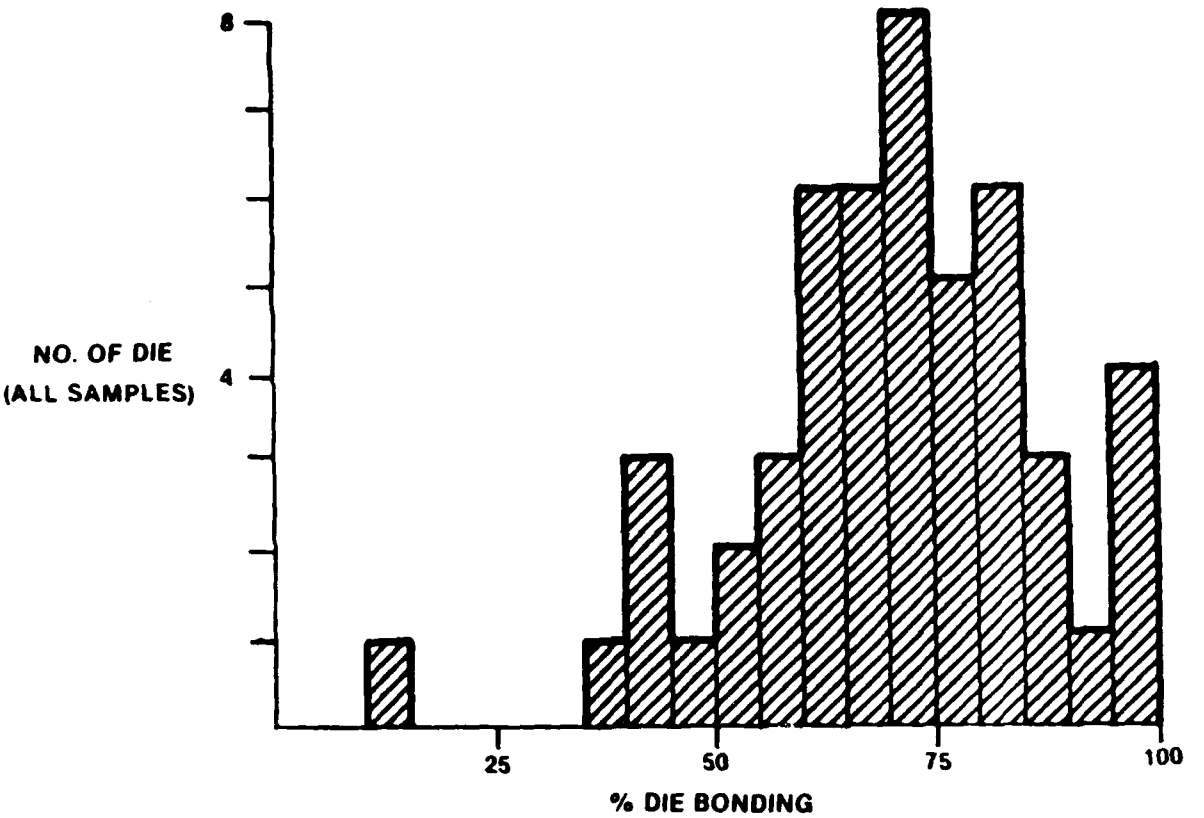


Figure 5.28 - Frequency distribution of percentage bonding for all samples.

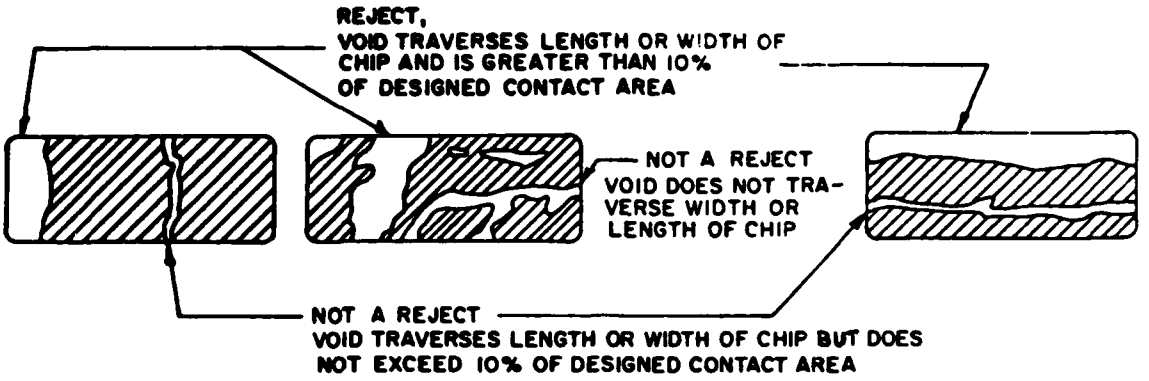


Figure 5.29 - Radiography die attach failure criteria.

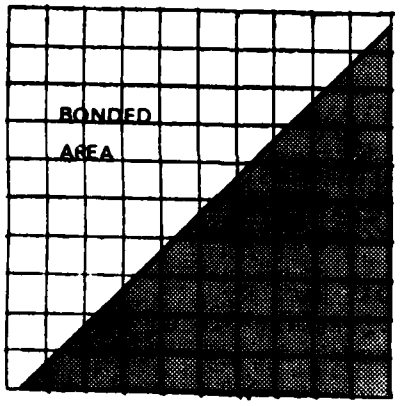


Figure 5.30 - Example of bonding material distribution which would be acceptable when judged by MIL-STD-883, Method 2012 (Radiography).

desirable bonding situation and would probably precipitate both severe adhesion problems (as in the case of our failed samples) and thermal management problems. In addition, as shown previously, the area of actual bonding may be much less than the total area covered by the bonding material as revealed by radiography. For the purpose of analyzing ultrasonic images, then, the radiographic failure criteria inadequately defined acceptable bond area distribution.

A total bond area minimum limit of 50 percent does appear to be reasonable. Eighty-eight percent of our samples were measured at greater than 50 percent bonded. However, one of the failed samples was 53 percent bonded, so some additional specification of bond material distribution is necessary.

Both samples which failed, fractured over a large corner void. Several other samples with comparable total bonding area and large voids, mainly enclosed by bonded regions, did not fail environmental stress testing. An initial ultrasonic image of a sample of this type is shown as Figure 5.31. This sample was bonded with a polyimide, and shows many unbonded areas, as well as a large enclosed void in the upper left corner of the image. From this and similar images, it appears that samples with large voids are most susceptible to mechanical failure when the void extends completely to the corner of the die. This conclusion is also supported by at least one known study[1]. Therefore, it was decided that the maximum limit on the size of a corner void should be 10 percent of the total intended contact area. This limit is slightly smaller than the corner area delineated by connecting the midpoints of the two edges of the die which form the corner in question. A corner void is formally defined for this purpose as a single, continuous void which extends under exactly two contiguous edges of the die and includes the corner of the die formed by the edges. All other types of voids were treated separately, as discussed below.

It has also been demonstrated that large contiguous voids severely degrade the thermal transfer characteristics of the die attach[2]. If a minimum total bonded area of 50 percent is to be allowed, the literature seems to

[1]Chiang, Steve S. and Shukla, Rama K.
"Failure Mechanism of Die Cracking Due to Imperfect Die Attachment"
Package Technology Development
Intel Corp.
1984 IEEE

[2]Mahalingam, M., et. al.
"Thermal Effects of Die Bond Voids in Metal, Ceramic, and Plastic Packages"
Semiconductor Research and Development Labs
Motorola, Inc.
1984 IEEE

Figure 5.31 - Ultrasonic image of die bonded with polyimide. Large void in upper left area comprises approximately 30 percent of total intended contact area. This sample did not fail environmental testing.

indicate that a reasonable maximum limit for the size of a single, contiguous void would be around 15 percent of the total intended contact area. An analysis of void size versus thermal degradation was not conducted for this study, however, so this test criteria should be evaluated through further study.

While it is desirable to keep the pass/fail criteria as simple as possible for any test method, some further limitations of bonding distributions seemed necessary, especially in the case where a sample marginally satisfies the other criteria. In cases where die scrubbing produces thin rivulets of bonding material barely separating moderate-size voids, for example, some further quantification of the distribution was necessary. A simple symmetrical scheme is to divide the image into four equal-sized quadrants by connecting the midpoints of opposite edges of the die image. In both of our failed samples it can be seen that this will produce one quadrant that is almost totally unbonded. While it is likely that such a quadrant will have a 10 percent corner void or a 15 percent edge or internal void, this is not necessarily the case. In such a case, a 15 percent (of the total die area) internal void would comprise 60 percent of the quadrant's area. A reasonable expectation seems to be that each quadrant should be at least 30 percent bonded for both adhesion and thermal purposes.

Conclusions

It is immediately obvious, when attempting to quantify the bond area distribution, that the effort is ideally suited for automated image inspection. At this time, however, the equipment to do this, while available, is not incorporated into existing ultrasonic imaging equipment to any sophisticated degree. In addition, constructing an algorithm which quantifies all image features is not a trivial task; neither is the task of deciding which configurations of image features constitute an acceptable die attach, and which do not. The above criteria, then, are offered as a simple manual means of quantifying ultrasonic image features, and assessing the contributions of various image features to the overall quality of the die attach.

A 100-square grid representation of the "worst case" distribution that would be passed by the criteria proposed above is shown in Figure 5.32 and appears, while not very desirable, at least more acceptable then the worst case passed by the present radiographic failure criteria: For this reason, it is also proposed that the pass/fail criteria of radiographic die attach void detection be changed to the proposed ultrasonic criteria.

The issue of damage during testing using ultrasonics on hermetic semiconductor devices should be addressed. Two factors of ultrasonic imaging may affect the integrity of the sample; the immersion of the sample in coupling fluid (distilled water), and the exposure of the semiconductor to ultrasonic energy.

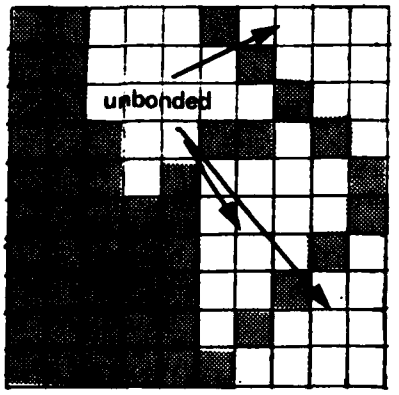


Figure 5.32 - 100-square grid representation of the "worst case" ultrasonic image which would pass the criteria recommended in the text for this method.

The frequency of the acoustic wave used to image our samples was 100 MHz. At this frequency, the energy associated with the wave is very low; many orders of magnitude below the energies used in ultrasonic cleaners, for example. For our samples, the intensity of the beam at the chip carrier back surface was approximately 8.0×10^{-7} W/in.^{2} of target, focussed on 1.8×10^{-4} in.^{2} of target at any one instant. As a result, the maximum estimated deflection of the area of chip carrier under the influence of the beam is approximately 2.4×10^{-7} in., roughly one-quarter of a micro-inch. The effect of the wave on the die itself will, of course, be even smaller.

From this information, it seems unlikely that the ultrasonic energy itself will adversely affect either the hermeticity of the package (by damaging seals, etc.) or the active surface and interconnections of the die. In the interest of completeness, however, it is recommended that the effects of ultrasonic imaging on the functional performance of active devices be evaluated.

If it is assured that the ultrasonic imaging process will not degrade the hermeticity of a device, then external package corrosion becomes the chief concern of submerging the device in a coupling fluid. At maximum spatial resolution (which requires the longest total scan, thus immersion, time) a device being ultrasonically imaged may be immersed for approximately 5 minutes. Using a clean immersion tank, distilled deionized water or an inert liquid as a coupling fluid, and rapid, thorough drying of the package will all minimize the possibility of package degradation or termination corrosion. Again it is recommended that the effects of ultrasonic imaging on external package features be evaluated in a future study.

RECOMMENDATIONS

The following recommendations are made from the results of Task 5:

- Perform further study to insure that the ultrasonic imaging process does not compromise the reliability of the devices under test.
- Include the Ultrasonic Imaging of Die Attach method as part of MIL-STD-883.
- Change the failure criteria of the Radiographic method (Method 2012) to those of the proposed Ultrasonic Imaging method.

TASK 6: TRANSMISSION PERFORMANCE

OBJECTIVE

The purpose of this task is to devise a test method to measure the electrical effects of packages on the transmission of VHSIC signals. Effects include signal degradation (due to ringing, attenuation and other transmission line effects) and propagation delay.

METHOD

Figure 6.1 is the classical model of the circuit elements of a transmission line. Prior work at Raytheon successfully used this model to predict IC to IC transmission performance through various transmission media including multilayer printed circuit boards and hybrid microcircuit substrates. Data for the calculation of circuit performance were gathered using a Time Domain Reflectometer (TDR), with special interface fixtures. The TDR can measure both the impedance and electrical length of the transmission media.

Circuit simulations using IC modelling data and the measured transmission line L/C/R/τ values were performed in SPICE 2 or an equivalent in-house simulator known as RAYCAP. Figure 6.2 is a typical output from this simulation process showing the propagation delay time and voltage waveform distortion predicted for one type of transmission line/logic family.

The approach taken in this study was to employ similar methods of TDR data gathering, with improved interface fixtures, to gather transmission parameter data on the various VLSI/VHSIC package types and configurations. Development of simplified calculations for determination of the relative performance of different packages and logic families was also attempted.

In an effort to achieve a simpler technique for package transmission performance measurements, a second method using the HP 4275A Multi-Frequency LCR Meter for direct L and C measurements was evaluated. However, the results were disappointing. No practical method could be found for reduction or elimination of series inductance in the ground return path when measuring package parameters. This stray inductance caused errors of 50% to 100% of transmission line impedance values. The TDR technique remains the only practical technique for today's package styles.

In the future, when high frequency VHSIC circuits are placed in controlled-impedance packages, it may be practical to employ RF S-Parameter measurement systems as an evaluation tool. RF Network Analyzers with time-domain-pulse analysis software packages are in routine use today to evaluate microwave microstrip networks. Consideration was given to application of this capability to the evaluation of VLSI packages but the prediction was that

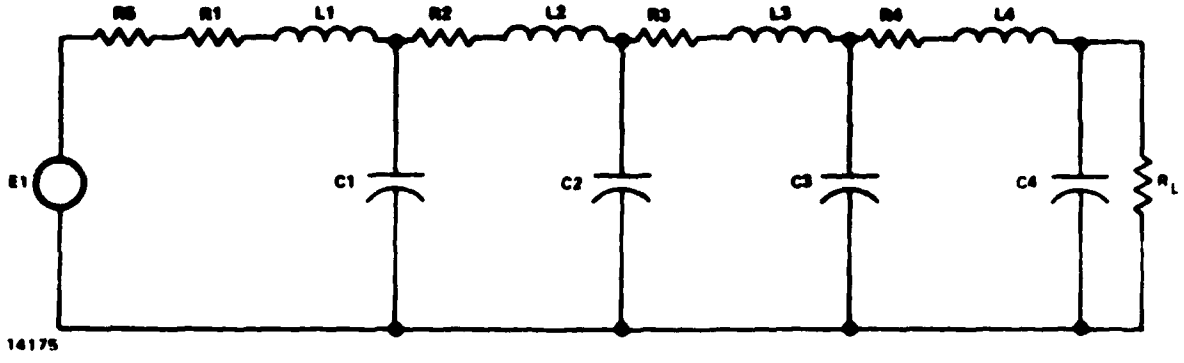


Figure 6.1 - Cascaded Lumped Parameter Model.

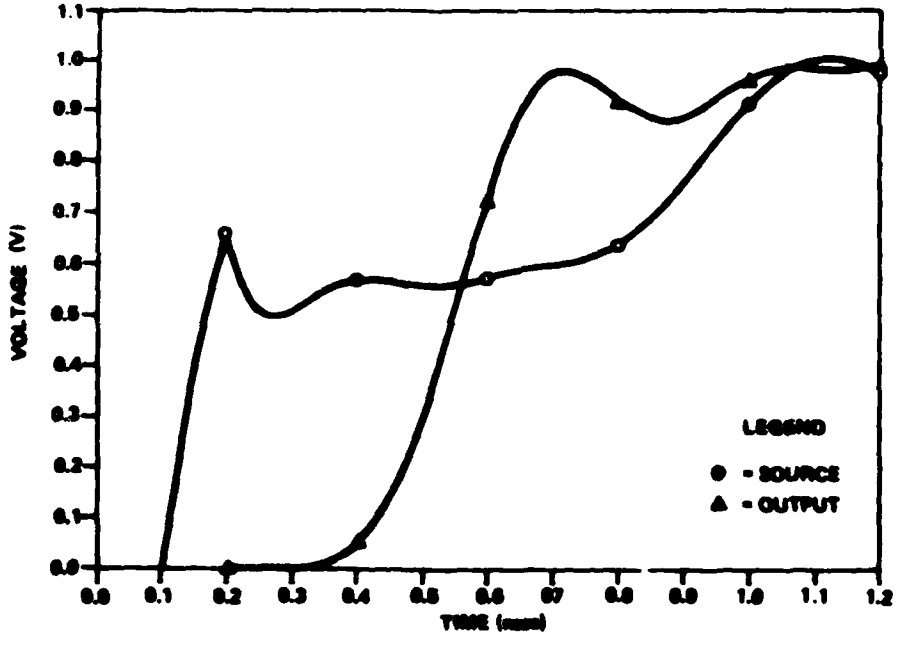


Figure 6.2 - Simulation of a Classic Source-Terminated Transmission Line.

performance would be no better than a TDR and interface fixturing is very difficult and expensive to design. Network Analyzers perform best in a 50-ohm environment and in that environment yield much better data than a TDR. However, in the typical VLSI package, impedances can vary from 20 to 200 ohms and standard S-parameter techniques cannot be used with good accuracy.

The TDR technique also has its limitations. The transmission line runs in many styles of packages are quite short. The TDR has a finite limitation in its ability to measure impedance changes over very short distances due to the rise time of the pulse generator (approximately 35 picoseconds) combined with the response time of the oscilloscope. Since the electrical length of a typical leadless chip carrier (CC) type package may be as short as 60 picoseconds, the TDR presentation tends to round out and average the impedance reading for these short transmission lines. It becomes a problem to locate the exact start and end of a transmission line section. Interpolation of impedance readings is necessary to account for the rise time of the measuring system. However, since the rise time of the TDR technique is still approximately 10 times faster than the fastest logic families being used in these packages, the technique is capable of providing data that is valid.

Figure 6.3 illustrates the difficulty in interpreting results. This is data for an 84-pin CC package which has lead lengths of approximately .25". Figure 6.3(a) shows a compressed scale view of the entire measurement setup. The line is terminated in an open circuit. Resolution is good and reflection due to the various transitions in the test setup can be identified. Figure 6.3(b) shows an expansion of the data from the package run at 50 ps/div. Figure 6.3(c) shows the same section at maximum expansion (20 ps/div). To get an accurate reading of electrical length, it is necessary to recognize that the actual start of the line section will appear 30-40 ps later than the step in the waveform and the end of the line will appear 20-30 ps prior to continuation of the step up towards the open circuit reflection value. Evaluation of impedance values also requires some interpolation but is not as difficult. In this case,the line is so short that it can be assumed that the data is affected by the oscilloscope bandwidth and TDR pulse rise time. The point marked "start" is actually at a slightly higher impedance level than the display indicates and the part marked "end" is at a slightly lower value. The average value is probably accurate in this case because the line was relatively long. For shorter sections, a lower-than-actual impedance value would be obtained for lines > 50 ohms and a higher-than-actual impedance value would be obtained for lines < 50 ohms.

The data gathered using the TDR method is reflection coefficient (ρ) vs. unit length propagation delay (τ). From these parameters the impedance of the transmission line can be calculated. This can be done either for an average for the entire line or for any point along the line from the formula:

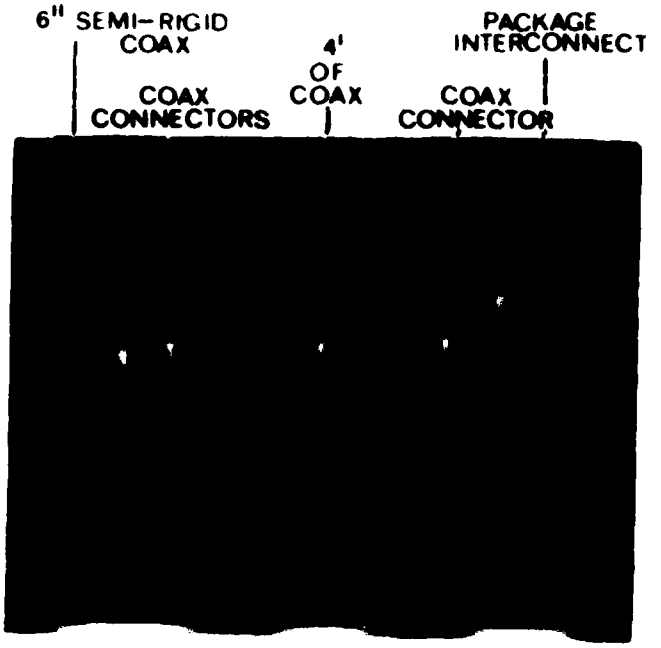


Figure 6.3(a)

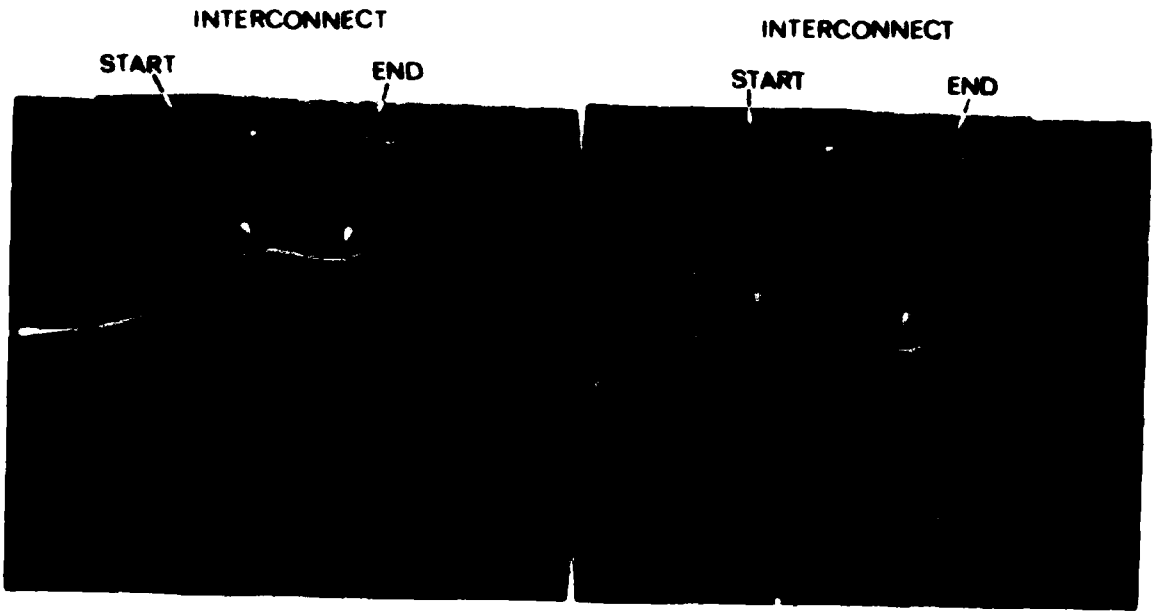


Figure 6.3(b)

Figure 6.3(c)

Figure 6.3 - TDR Results for 84 I/O leadless Chip Carrier.

$$Z_0 = \frac{1 + \rho}{1 - \rho} \cdot Z_{Ref}$$

Where Z_{Ref} = the nominal impedance of the reference transmission line leading up to the package being tested. It is best to use a reference line value nearest that of the package being tested (e.g., for a 100-ohm typical package, use a length of 95-ohm coaxial cable instead of conventional 50-ohm cable). This reduces the error caused by the rise time of the TDR system. Figure 6.8 demonstrates this effect. A package pin in the 100-ohm range is measured using both 50-ohm and 95-ohm test fixture cables. A reading approximately 8 ohms higher is obtained using the 95-ohm cable.

T is a direct reading of the time delay between the points identified as the "start" and "end" of the package transmission line section.

From the readings and the package physical dimensions the following circuit values can be derived (refer to the TDR data in Figure 6.3(c)):

$$\tau = \frac{\text{Measured Delay (T)}}{\text{Measured Length (inches)}}$$

$$R_\ell = \frac{\text{Measured R}}{\text{Measured length (inches)}}$$

$$C_\ell = \frac{\text{Capacitance}}{\text{Unit Length}} = \frac{\tau}{Z_0}$$

$$L_\ell = \frac{\text{Inductance}}{\text{Unit Length}} = \frac{\tau^2}{C_\ell}$$

Values of C_n and L_n for the cascaded lumped parameter model of Figure 6.1 are calculated for the "start", "end" and "mid" values of measured Z_ℓ observed on the TDR and applied to the respective C_1, C_2 and C_3 stages of Figure 6.1; similarly, L_1, L_2 and L_3 are calculated and applied to the model. C_4 is the IC input capacitance. Values of R_n are obtained by measuring the DC resistance of the line (see Task 9) and calculating the R_ℓ.

Modelling the transmission line together with IC parameters in SPICE 2 allows an accurate evaluation of the effect of the package parameters on pulse waveshape and propagation delay. These values can also be used in the larger model of the entire printed wiring board environment.

It is not necessary to model the exact performance of the package and IC combination to evaluate the match of average package impedance to the source and load impedances it "sees" in its application environments. This is similar to the "VSWR" matching concept used in RF systems. The impedance in digital circuits, especially of drivers, changes non-linearly over wide ranges during "1" to "0" transitions. In RF circuits impedance is a constant value, usually 50 ohms.

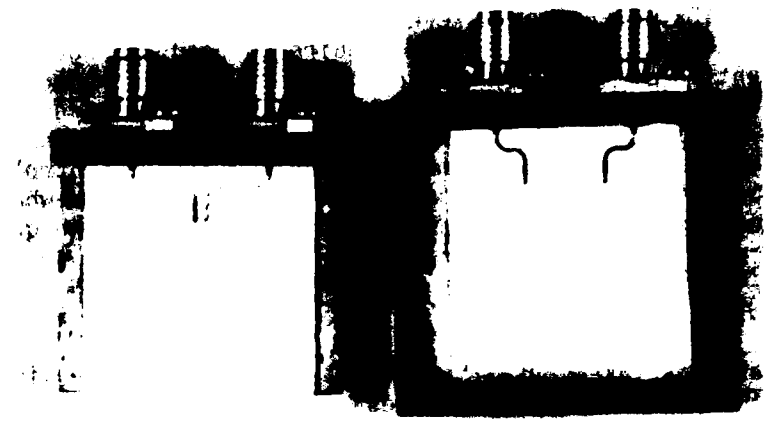
Work remains to be done to determine what constitutes the allowable impedance mismatch value range for digital circuits. Certainly it varies among different logic families.

Meanwhile, TDR data is useful for evaluating which packages fall between the impedance value range for a given logic family and which are outside. For example, if a logic family has a drive impedance value of 120 ohms in the "1" state and 50 ohms in the "0" state, a package with a line impedance value in the 80 to 100 ohms range seems a good compromise whereas a 150-ohm line may not be.

Time Domain Reflectometry (TDR) has been the technique used in evaluating transmission performance. The TDR used consisted of a 7S12 plug-in to the Tektronix 7904 scope, using an S-52 pulse generator and an S-6 sampling head. The risetime of the pulse produced by the TDR is less than 35 ps. Because the TDR is a high frequency device, and works in a 50-ohm environment, fixturing required special attention.

Initial efforts of soldering a 50-ohm coaxial cable, stripped back on one end, directly to the package were unsuccessful with certain package types (leadless chip carrier, pad grid array). The high inductance of the stripped-away portion of the coax induced error with these packages. The mechanical interfacing was extremely tedious and many times connections were not good enough to work with the packages. However, this method proved sufficient for the pin grid array and leaded chip carrier type packages. The error induced in these packages was negligible compared to the highly inductive length of exposed package leads.

A 50-ohm microstrip fixture (Figure 6.4) was built to interface with three package types: leadless chip carrier, pad grid array, leaded chip carrier. The electrical connection between the fixture and the package was either by pressure contact or by solder connection. This method produced minimal front end mismatch error in taking TDR measurements.



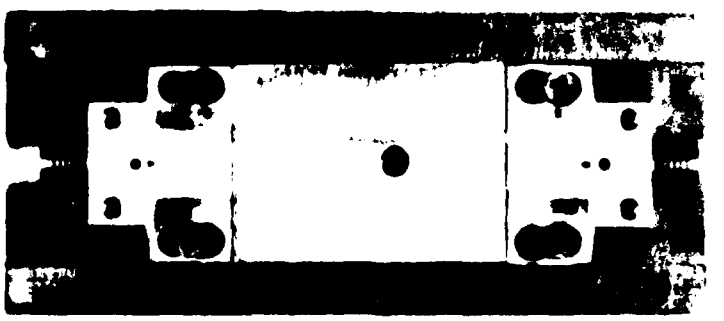


Figure 6.4 - 50-ohm microstrip fixtures.

Initial TDR measurements were made using 50-ohm terminating resistors inside the package. This technique required a good package ground plane, not always present in some package styles. Errors were introduced by the length of package wiring between the ground and the terminating resistor. A simple solution to this problem was to use an open-circuited terminator. This technique requires some readjustment of the TDR offset controls and increases the amount of noise and reflections on the TDR display somewhat, but these problems caused much less distortion to the signal than the grounding problems encountered with matched termination resistors.

RESULTS

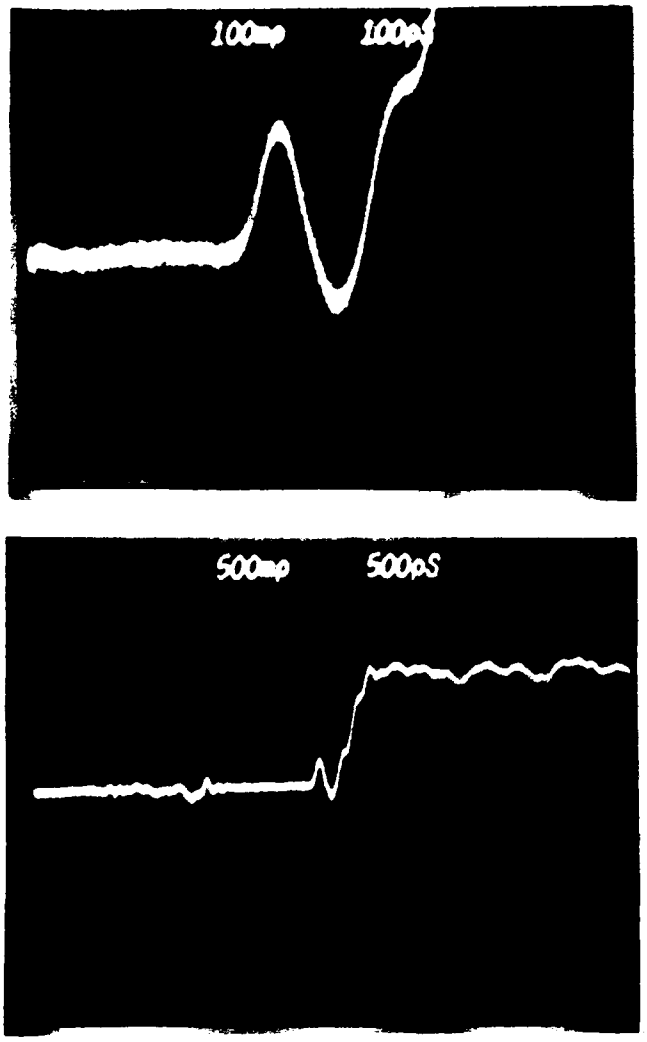
TDR data was taken on all package types and is listed in Table 6.1. The sample TDR photos shown in Figures 6.5 through 6.9 were the source for the data except for R which was measured using the DC resistance measurement techniques described in Task 9.

The TDR measurements were made using the transmission line interfaces described above; a 50-ohm stripline fixture for leadless and pad grid package styles and a coaxial cable interface to the pin grid and leaded packages styles. The interfaces were refined to minimize the transition mismatch due to the fixture transmission line interface being of a different characteristic impedance at the point just prior to the physical solder joint to the package. This is not a problem with the stripline fixture but it is difficult to achieve with a coaxial cable interface. If there is a transition mismatch near the interface to the package, significant data errors will be experienced, especially on short package runs. This is due to the limited time resolution of the TDR system. Transient peaks near the interface will blend in with the reflection data from the first 20 to 30 picoseconds of the package run, causing errors.

Table 6.1 - Transmission Line Data

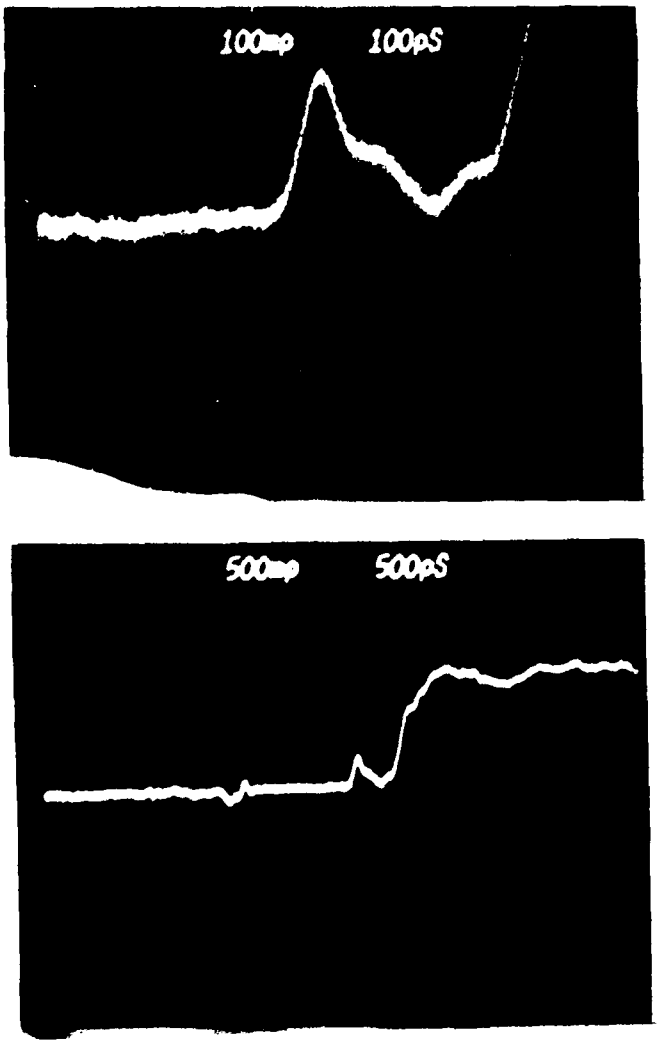
Package	Z_{ave}	C	L	τ	R
84 I/O Pin Grid	55 Ω	1.8 pf	5.5 nH	100 ps	245 mΩ
180 I/O Pad Grid	74 Ω	4.26 pP	14.67 nH	250 ps	245 mΩ
144 Leadless CC	78 Ω	3.39 pf	9.56 nH	180 ps	485 mΩ
64 Leaded CC (.375 Cavity)	94 Ω	0.63 pf	5.7 nH	60 ps	325 mΩ
64 Leaded CC (.344 Cavity)	87 Ω	0.57 pf	4.39 nH	50 ps	355 mΩ

An evaluation of the quality of the fixture interface can be made by soldering a small 50-ohm chip resistor between the interface and the fixture ground plane in the exact same configuration and position as the package



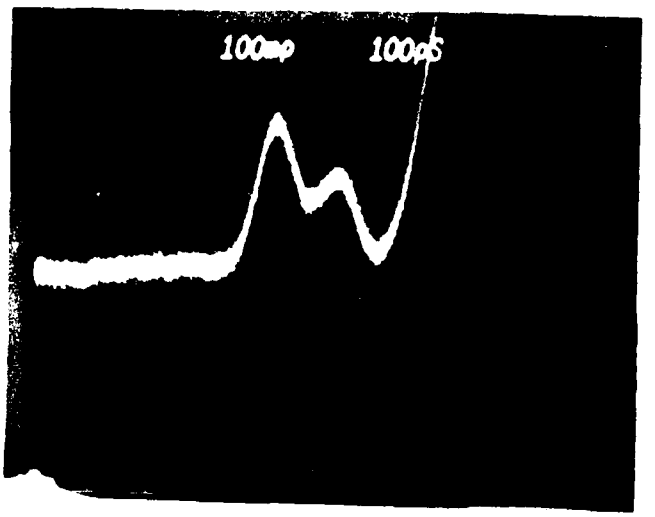
ρ_{max} = 0.2 Z_{max} = 75Ω
ρ_{min} = 0.1 Z_{min} = 41Ω
ρ_{ave} = 0.05 Z_{ave} = 55Ω
T = 100 pS
C = 1.8 pf
L = 5.5 nH

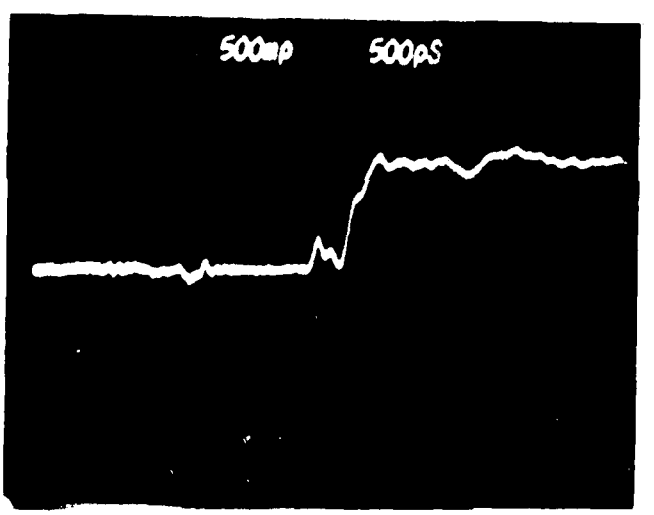
Figure 6.5 - TDR Response of 84 I/O Pin Grid Array.



ρ_{max} = 0.30 Z_{max} = 92.9Ω
ρ_{min} = 0.08 Z_{min} = 58.7Ω
ρ_{ave} = 0.19 Z_{ave} = 73.5Ω
T = 250 pS
C = 4.26 pf
L = 14.67 nH

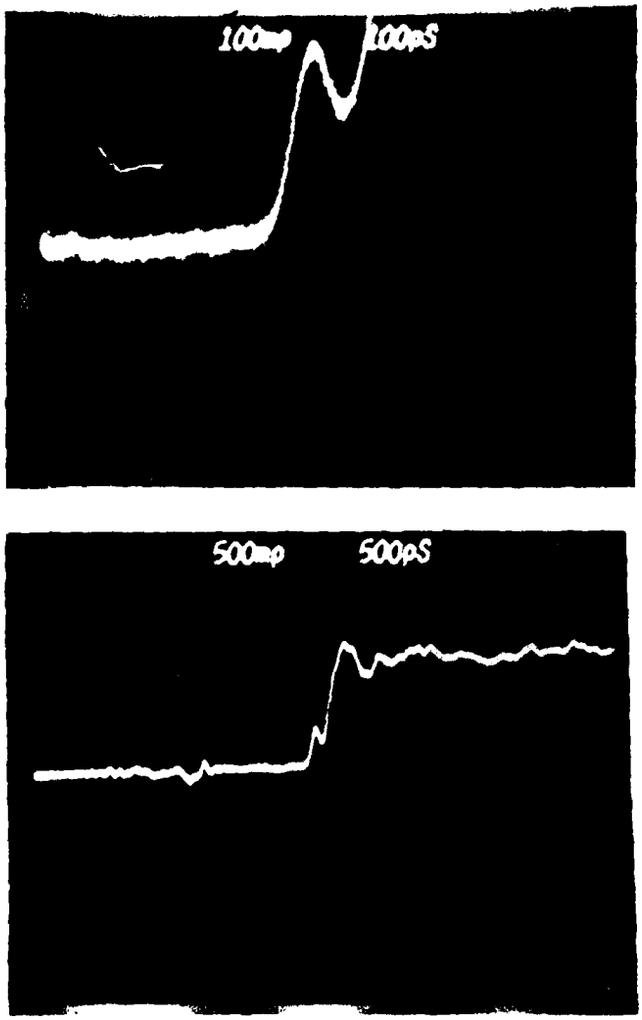
Figure 6.6 - TDR Response of 180 I/O Pad Grid Array.





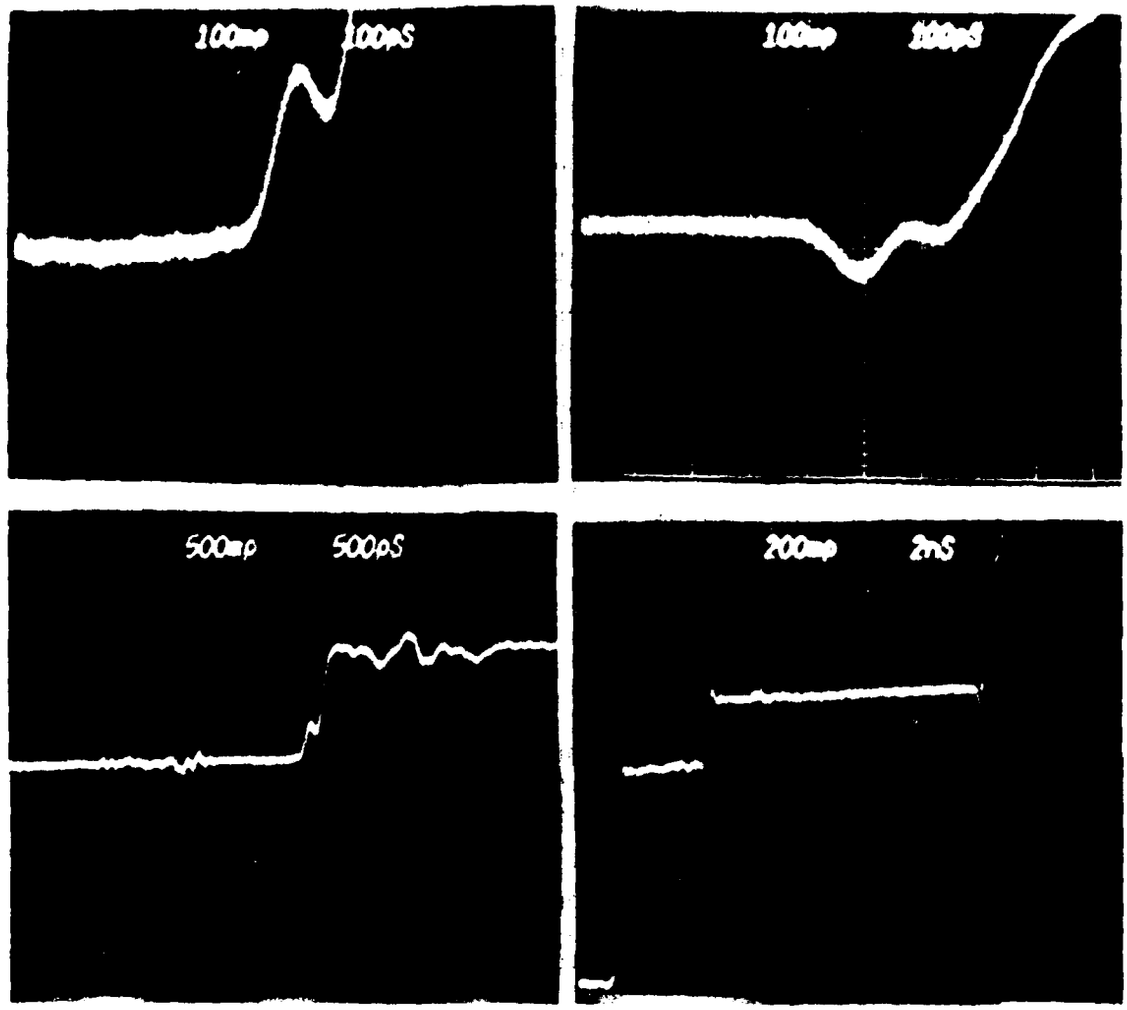
ρ_{max} = 0.24 Z_{max} = 81.6Ω
ρ_{min} = 0.03 Z_{min} = 53.09Ω
ρ_{ave} = 0.135 Z_{ave} = 78.03Ω
T = 180 pS
C = 3.39 pf
L = 9.56 nH

Figure 6.7 - TDR Response of 144 I/O Leaded Chip Carrier.



ρ_{max} = 0.360 Z_{max} = 106.25Ω
ρ_{min} = 0.250 Z_{min} = 83.3Ω
ρ_{ave} = 0.305 Z_{ave} = 93.9Ω
T = 60 pS
C = 0.63 pf
L = 5.7 nH

Figure 6.8 - TDR Response of 64 I/O Leadless Chip Carrier (0.375 Cavity).



a. 50 Ω interface

ρ_{max} = 0.30 Z = 92.5Ω
ρ_{min} = 0.24 Z = 81.6Ω
ρ_{ave} = 0.27 Z = 86.98Ω
T = 50 ps
C = 0.57 pf
L = 4.39 nH

b. 95 Ω interface

ρ_{max} = 0.40 Z = 102.9Ω
ρ_{min} = 0.04 Z = 87.7Ω
ρ_{ave} = 0.0 Z = 95Ω

Figure 6.9 - TDR Response of 64 I/O Leadless Chip Carrier (0.344 Cavity).

interface. This will enable a TDR presentation of the magnitude of the pre-transition mismatch which must be minimized by correct design of the transmission line interface and package-mounting schemes.

When measuring the package parameters with the TDR, best results were obtained looking into the package-with-the-package run/chip-interface media left unterminated in an "open-circuit" configuration. The chip-to-package interconnect should be arranged to duplicate actual conditions by bonding to a chip pad which is totally isolated from chip circuitry or in the case of a wirebond interconnect, arcing the bond in the approximate location above the package ground plane that would be experienced in an actual interconnect.

The TDR data in Figures 6.5 through 6.9 shows two-scale presentations of the same test configuration. The 500 mρ/500 ps display shows the total test environment. The presentation in Figure 6.5, for example, shows the 50-ohm transmission line of the test fixture interface to the left of the centerline. The start of the package run is at the centerline and continues for approximately 100 ps when the transition to an open circuit ($\rho = 1$) occurs. The "steps" in the transition to the $\rho = 1$ condition are due to multiple "echoes" in the TDR setup and can be moved or eliminated by increasing the length of the coaxial cable between the TDR and the fixture. The measurement is referenced to the characteristic impedance of the coaxial cable by adjusting TDR offset controls so that the flat line to the left of center/horizontal is placed exactly at center/vertical. In this case, a $Z_{REF} = 50$ ohms is established. Other reference impedances may be established with various types of coaxial or stripline interfaces having other impedance values (the TDR may be used to calibrate the impedance of any adaptor).

The expanded scale photo (100 mρ/100 ps) is used to obtain the reflection coefficient and propagation delay data for the package. For very short package runs the 50 ps/scale in the TDR may be used. The apparent location of the exact start of the package run is affected by the rise time of the TDR system. Experimentation has shown that the TDR yields values of propagation delay that are typically 50 - 80 picoseconds larger than actual due to the rise time of the pulse and the slew rate of the oscilloscope. Errors are smaller for lines nearer the characteristic impedance of the test fixture because the oscilloscope beam does not have to slew as far for small values of ρ. For example the line of Figure 6.5 appears to start approximately 30 picoseconds after the centerline for a total length of 160 ps. Insertion of shorts, opens and 50-ohm chip resistors at either end of the line showed the line length to be 100 ps.

The impedance data of Table 6.1 are useful in an evaluation of the package's relative match of Z_{ave} to various logic families from low-impedance ECL to high-impedance CMOS. The parameters can also be inserted into the cascaded model of Figure 6.1 for pulse response analysis and prediction in SPICE 2. The method generally used is to calculate the maximum frequency of propagation (f_o) for the transition time (t_t) in the logic system as follows:

$$f_o = \frac{1}{2t_t}$$

Modelling of a transmission requires that a unit RLC "T" section be developed for each

$$\ell = \frac{\lambda}{4} \quad \text{where} \quad \lambda = \frac{c}{\sqrt{\varepsilon}\, f_o}$$

and c = velocity of light = 3×10^{10} cm/sec

and ε = effective dielectric constant of the package material (typical $\varepsilon = 8$ for ceramic)

For a ceramic package example with t_t = 500 ps:

$$f_o = \frac{1}{1000 \times 10\text{-}12} = 10^9 \text{ Hz}$$

$$\lambda = \frac{3 \times 10^{10}}{2.83 \times 10^9} = 10.6 \text{ cm}$$

$\ell = \lambda/4 = 2.65$ cm or 1.04 in. (t_t = 500 ps)

or 2.08 in. (t_t = 1 ns)

or 0.52 in. (t_t = 250 ps).

Therefore, for a 2-in. package run, a minimum of two "T" section models is required at t_t = 500 ps. For most applications, a three-section model is used. LC data are taken from the left, middle and right portions of the TDR display and inserted in the corresponding section of the model. Figure 6.10 is a typical SPICE input model used to predict performance of a CMOS driver/receiver pair. Figures 6.11 and 6.12 show the predicted response of this network for a pulse with a rise time (t_t) of 1 ns and 0.1 ns respectively using a CMOS integrated circuit model for drive and load impedance.

CONCLUSIONS

The TDR method of evaluating the transmission line impedance of package runs has been shown to be an effective technique for evaluating this important aspect of package performance. Great care must be exercised in the design of fixtures to interface the TDR to the package and in interpretation of the

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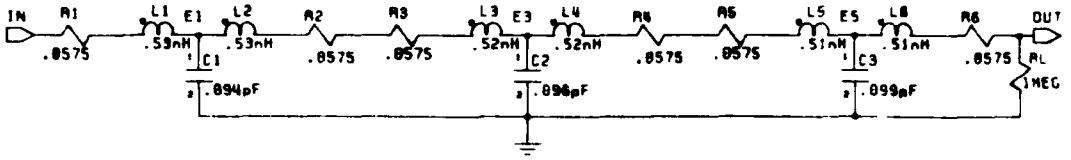


Figure 6.10 - Typical Package Network Cascaded Model.

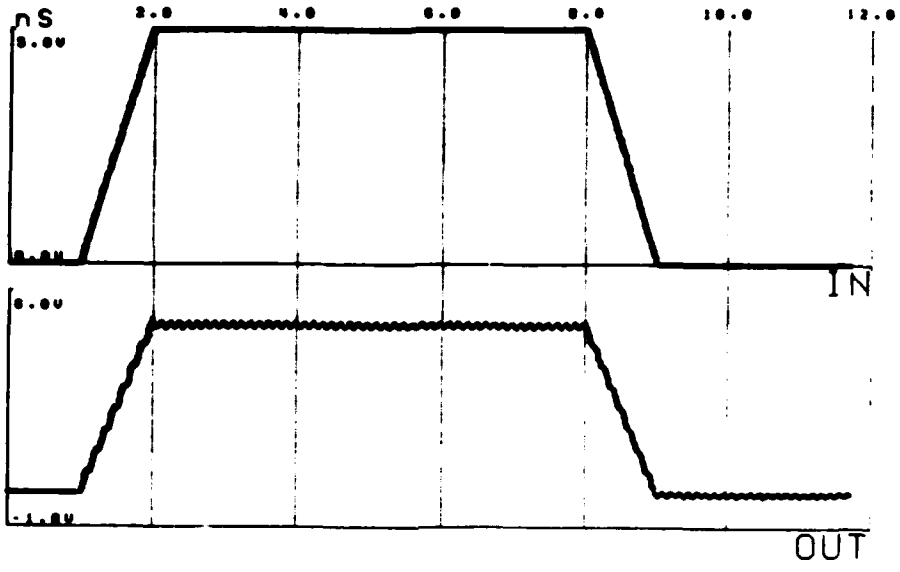


Figure 6.11 - Pulse Response t_t = 1 ns (Network of Figure 6.10).

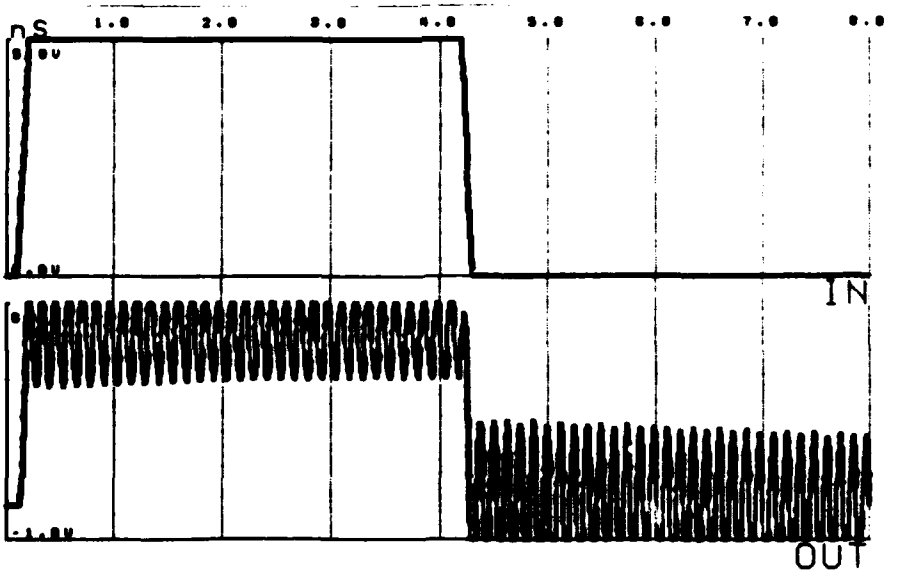


Figure 6.12 - Pulse Response t_t = 1 ns (Network of Figure 6.10).

TDR data. If this is done, the results yield data that would enable IC manufacturers to adjust package characteristic impedance for optimum performance at high frequencies. The data can also be used in SPICE 2 circuit simulations to predict IC performance. The technique will enable the evaluation of various packages and chip to package interface techniques.

RECOMMENDATION

- Include the Microelectronics Package Digital Signal Transmission method as part of MIL-STD-883 to aid in electrical evaluation of packages.

TASK 7: CROSSTALK

OBJECTIVE

The purpose of this task is to develop a test method that will measure a package's line-to-line isolation characteristics. A package must provide enough isolation so that false triggering of the input on a line does not occur when the adjacent line is pulsed. The noise immunity of digital circuits to sources of interference outside the package is also of concern as is the increase in time "jitter" due to crosstalk noise.

METHOD

Three different crosstalk measurement techniques were evaluated. The first method was RF S-parameter network analysis. This technique requires elaborate, precision test fixtures. These fixtures become part of the measuring system and any transmission line discontinuities or mismatches degrade the measurement capabilities of the system. Each package type would require its own fixture. In addition to the fixturing problem, the calculation of crosstalk for a given set of pulse characteristics proved so difficult that the technique was abandoned.

The second method was to measure capacitance between adjacent lines. Measurements of capacitance for various packages were made using the HP4275 multi-frequency LCR meter. The LCR meter's test points are isolated from ground and the measurement must be made with the lines unterminated. Consequently, this technique proved to be a poor approximation of normal operating conditions. The simple capacitive coupling model used in the calculation gave results that could not be validated by crosstalk measurements made using other techniques. Series inductance in the package leads affects the crosstalk coupling significantly and this method could not accurately account for this.

The third method was to drive a narrow (18 nsec) fast rise (< 1 nsec) pulse into a package line, terminated in 50 ohms. The cross coupling could be determined by monitoring an adjacent line terminated with various resistor loads. The measurements were made using an HP8082A pulse generator and an HP54100D digitizing oscilloscope with HP54001A, 10:1, 10Kohm 2pf probes. Six measurements were made on each package, each measurement with a different load. Miniature chip resistors were used. The loads were 10,000 ohm, 4990 ohm, 2000 ohm, 1000 ohm, 499 ohm and 249 ohm. The equivalent loads were 5000 ohm, 3330 ohm, 1670 ohm, 909 ohm, 475 ohm and 243 ohm because of the 10,000 ohm probe impedance. Figure 7.1 shows the test setup.

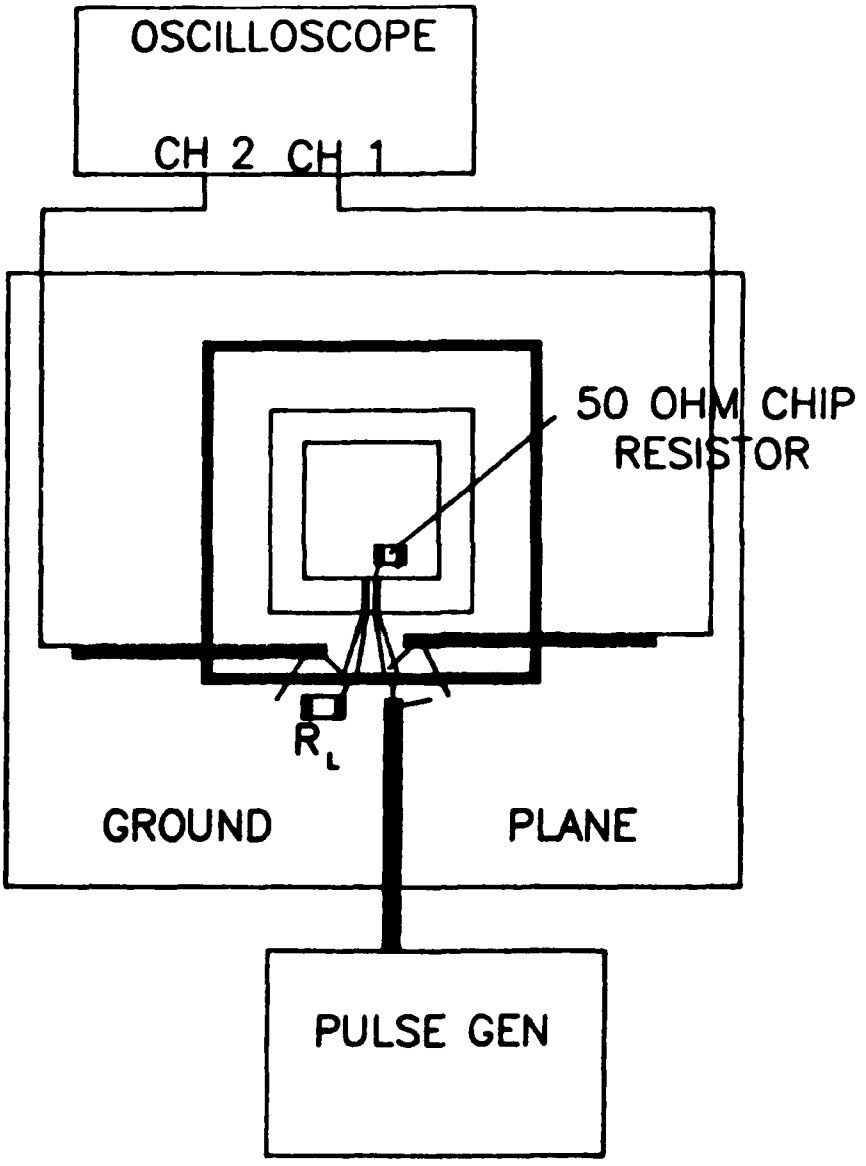


Figure 7.1 - Test Setup Schematic for Crosstalk Measurements.

The fixturing was not complex. Perforated type vector board, copper clad on one side, was used to provide a ground plane. The package was attached by soldering the internal ground to the ground plane through the package leads. The pulse was applied through a coaxial cable with the shield soldered to the ground plane and center conductor soldered to the driven pin. This pin was monitored by a 10:1 probe connected to channel 1 of the oscilloscope, the adjacent line, terminated with a resistor to ground at the package exterior was monitored by using another 10:1 probe connected to channel 2 of the oscilloscope. This measurement was repeated for the resistor values listed above. Four package types were measured.

RESULTS

The results of the test are shown in Figures 7.2 through 7.5.

From the data, it can easily be seen which package has the most cross coupling. A calculation can also be performed to determine the effective coupling capacitance. To do this, a load or a pulse width must be chosen which allows time enough for the coupling capacitance to charge completely. (The charge is complete when the pulse reaches 0V.) Then, by using the formula for RC time constant T=RC, calculate the time it takes for 63% of the charge to be completed. This time divided by the added resistance equals the total capacitance. By subtracting the test probe capacitance, the effective coupling capacitance can be obtained.

For example from the plot of the coupled signal on the 84 I/O pin grid package with a 909Ω load (Table 7.1; Figure 7.5(c)):

The peak voltage is 306 mV

$306(.63) = 192.78$

$306 - 192.78 = 113.22 = 63\%$ of the charge

$T = 7.75$ nsec

$$C_T = \frac{T}{R} = \frac{7.75 \times 10^{-9}}{909} = 0.0085 \times 10^{-9} = 8.5 \times 10^{-12} = 8.5 \text{ pf}$$

$C_T = C_C - C_P$ (C_C and C_P are in parallel during discharge)

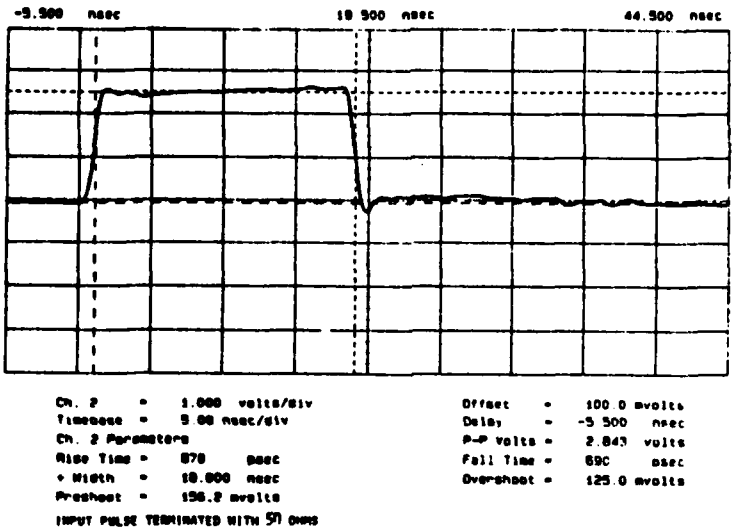
$C_C = 8.5\text{pf} - 2.0\text{pf} = 6.5\text{pf}$

Values for all the packages are given in Table 7.1.

Table 7.1 - CALCULATED COUPLING CAPACITANCE (C_C)

Package	V_{PEAK} (mV)	63% of the Charge (mV)	T (nsec)	C_T (pf)	C_C (pf)
64 I/O Leadless CC .375 CAVITY	210	77.7	3.0	3.3	1.3
64 I/O Leadless CC .344 CAVITY	225	83.25	4.8	5.3	3.3
84 I/O PIN GRID	306	113.2	7.75	8.5	6.5
180 I/O PAD GRID	263	96.9	8.3	9.1	7.1

LINES LOADED WITH 909 OHMS



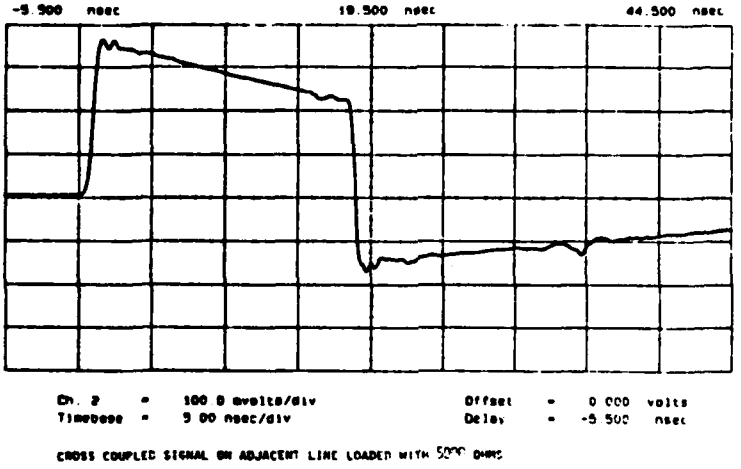
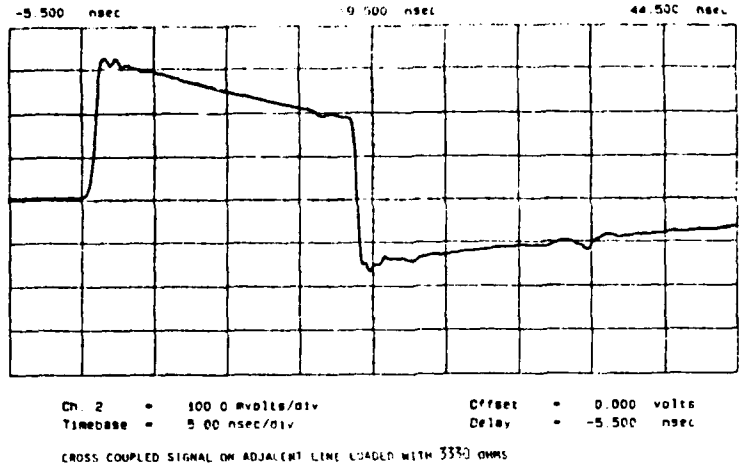


Figure 7.2(a) - Crosstalk As a Function of Load Resistance for 84 I/O Pin Grid Package.



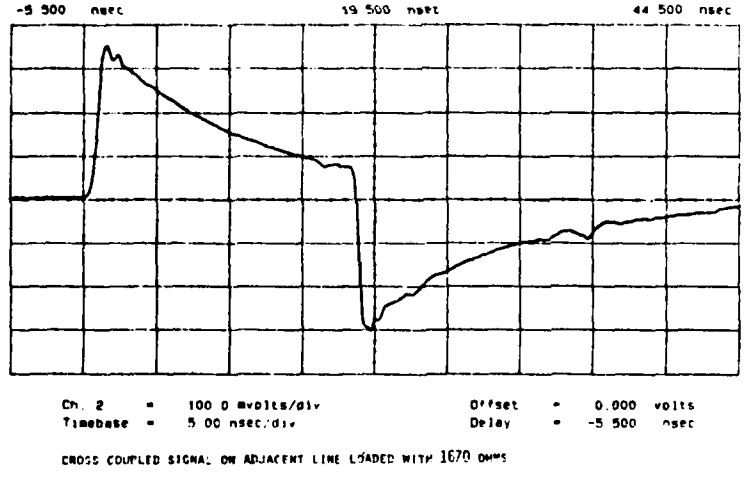
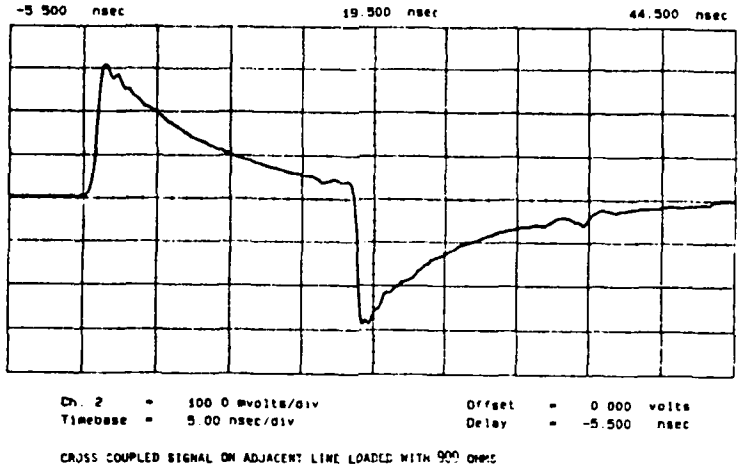


Figure 7.2(b) - Crosstalk As a Function of Load Resistance for 84 I/O Pin Grid Package.



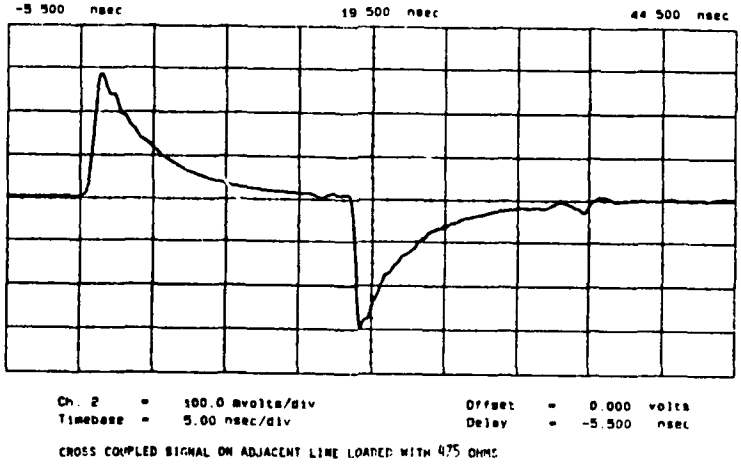


Figure 7.2(c) - Crosstalk As a Function of Load Resistance for 84 I/O Pin Grid Package.

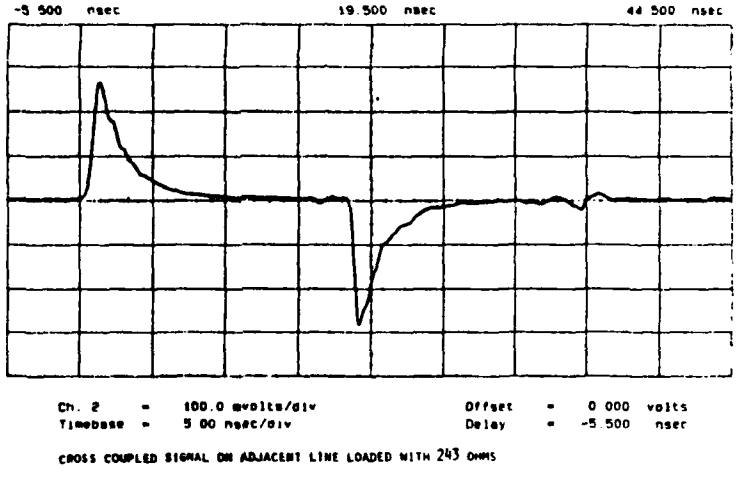
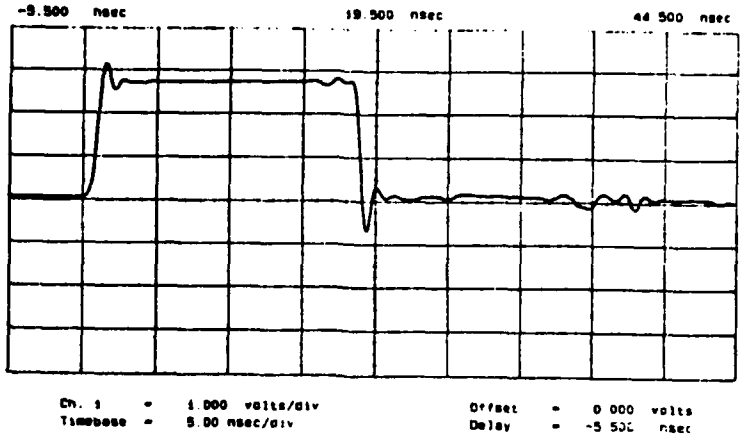


Figure 7.2(d) - Crosstalk As a Function of Load Resistance for 84 I/O Pin Grid Package.



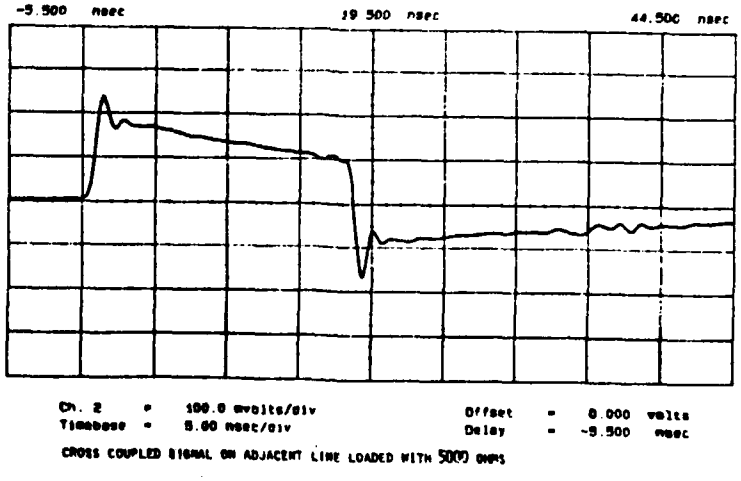
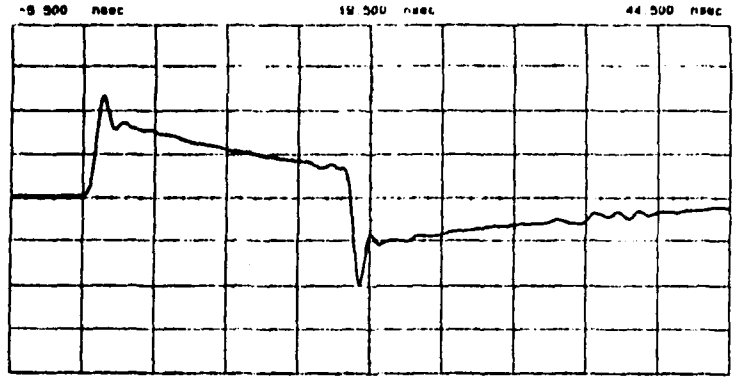


Figure 7.3(a) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.375 Cavity).



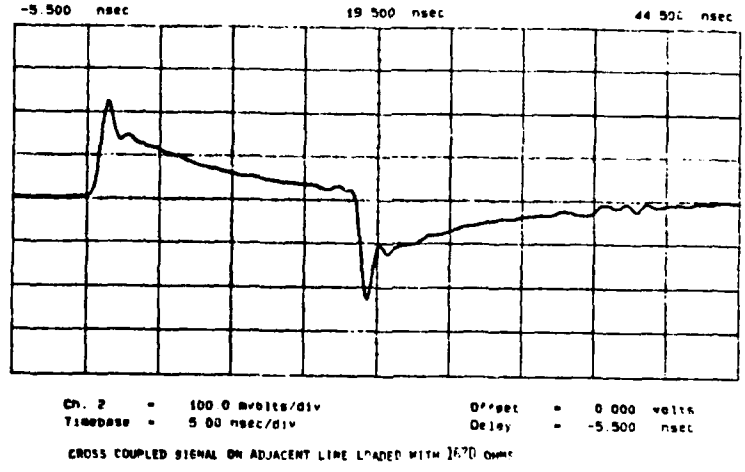
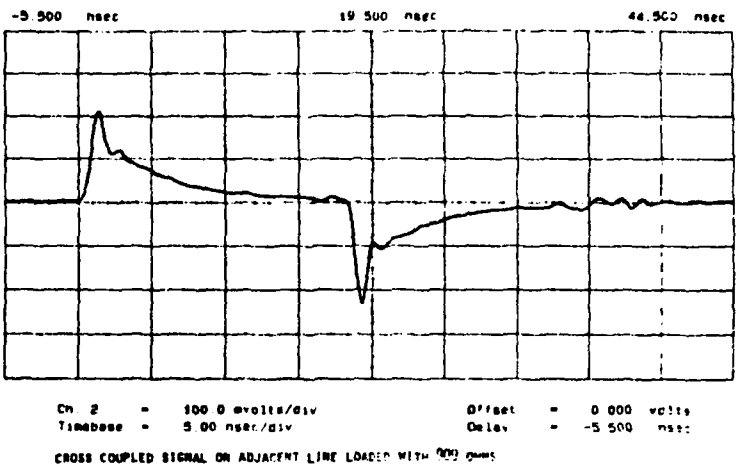


Figure 7.3(b) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.375 Cavity).



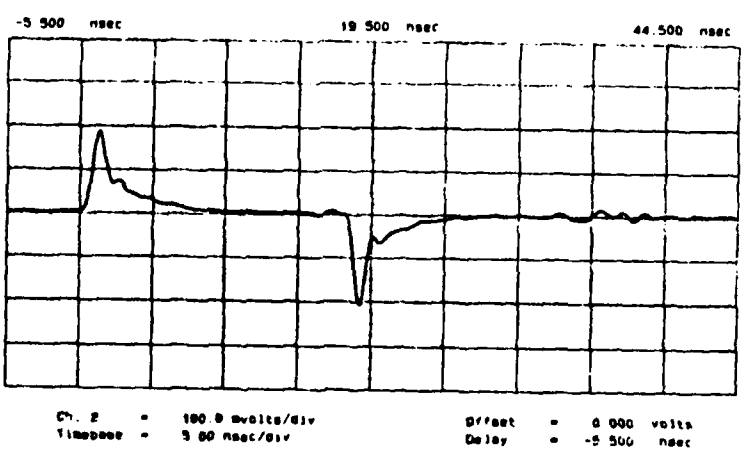


Figure 7.3(c) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.375 Cavity).

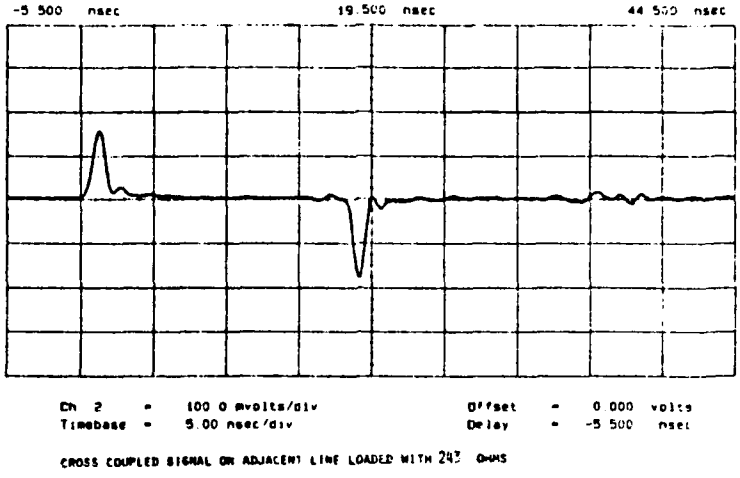
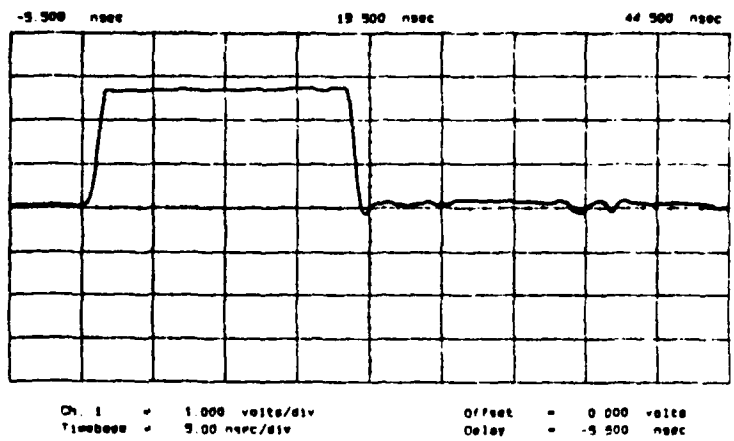


Figure 7.3(d) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.375 Cavity).



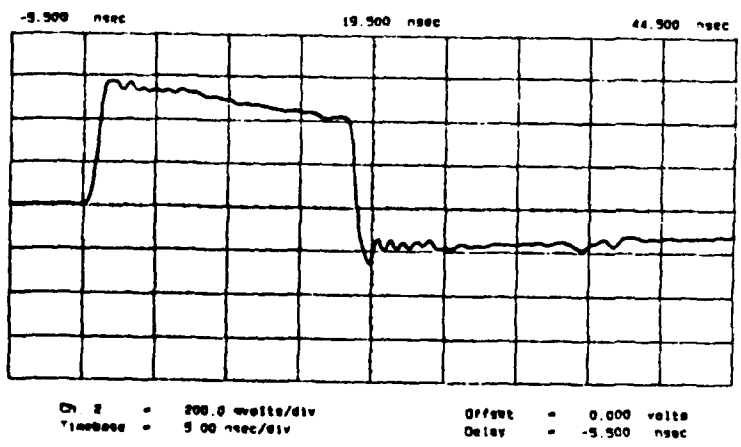
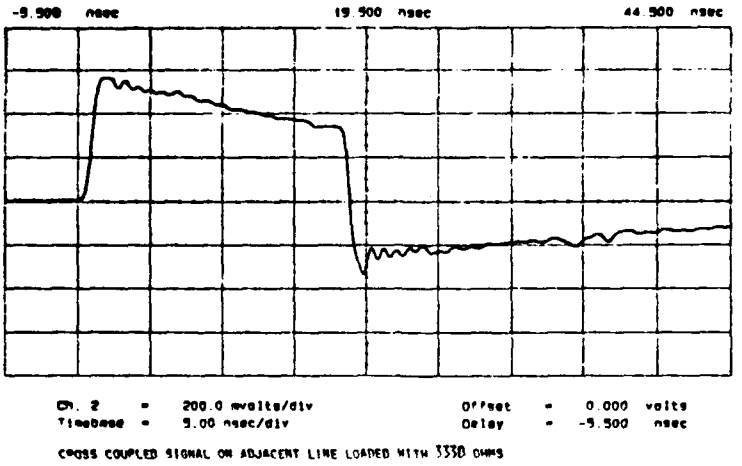


Figure 7.4(a) - Crosstalk As a Function of Load Resistance for 180 I/O Pad Grid Package.



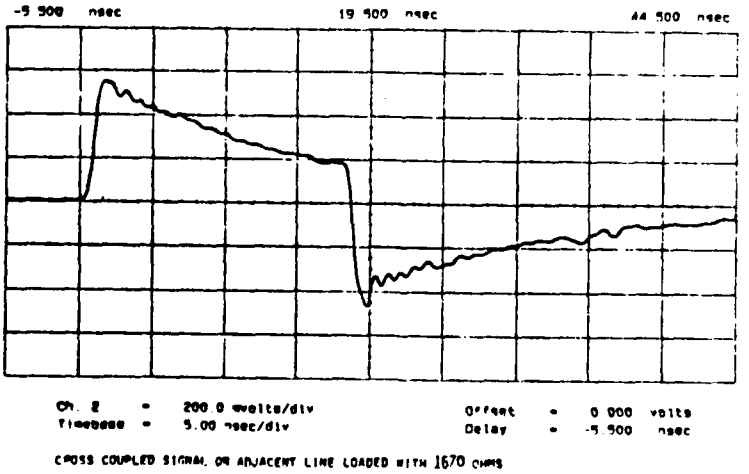
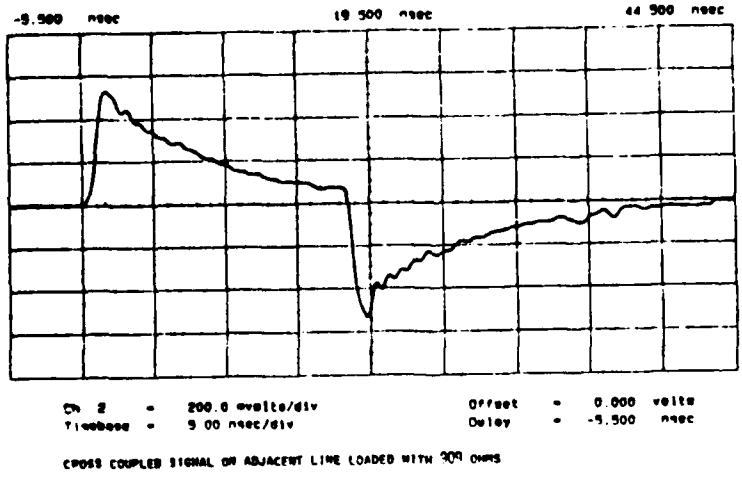


Figure 7.4(b) - Crosstalk As a Function of Load Resistance for 180 I/O Pad Grid Package.



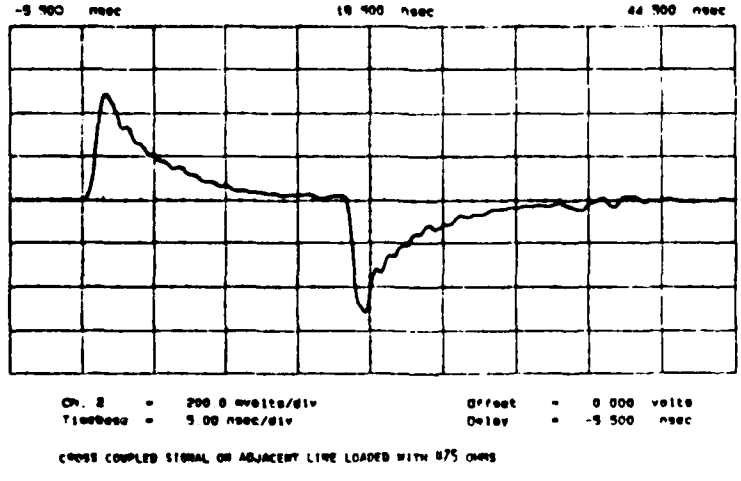


Figure 7.4(c) - Crosstalk As a Function of Load Resistance for 180 I/O Pad Grid Package.

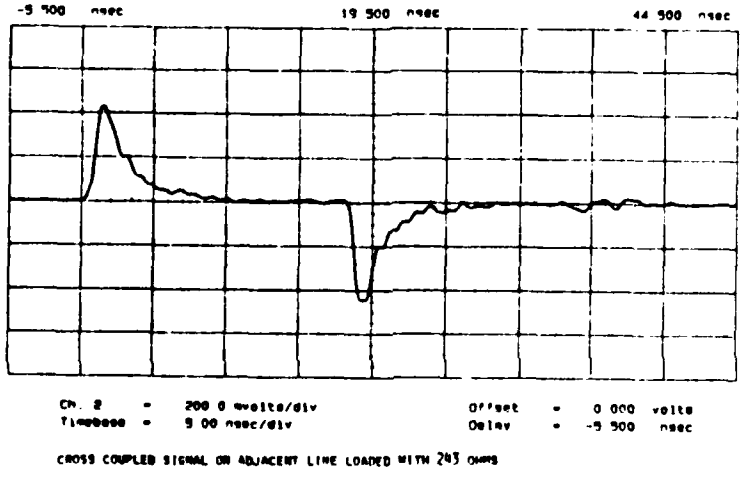
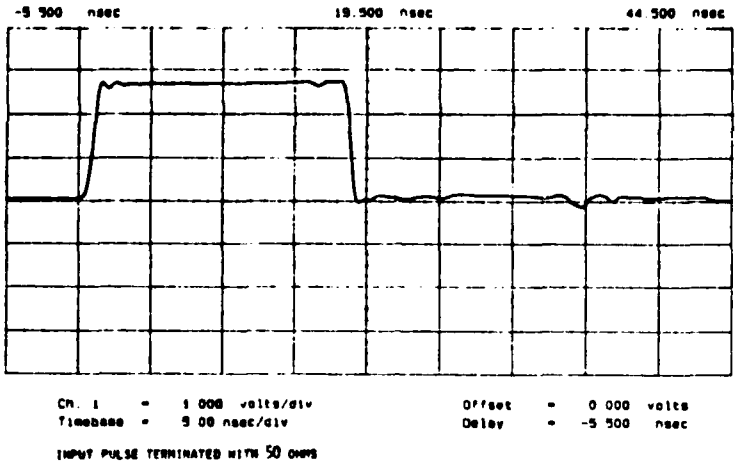


Figure 7.4(d) - Crosstalk As a Function of Load Resistance for 180 I/O Pad Grid Package.



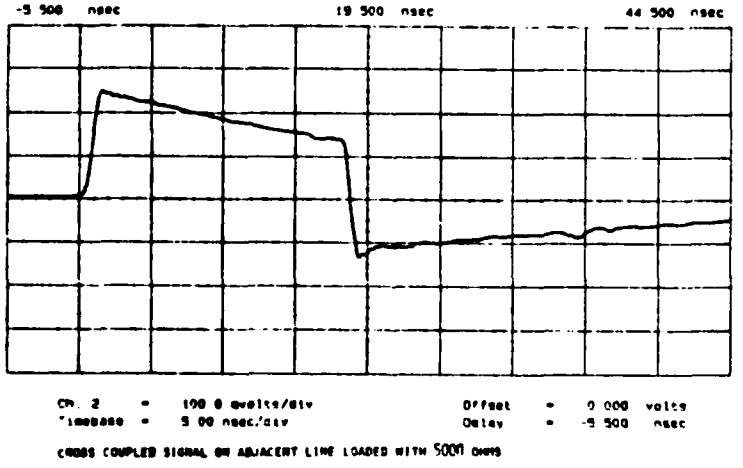
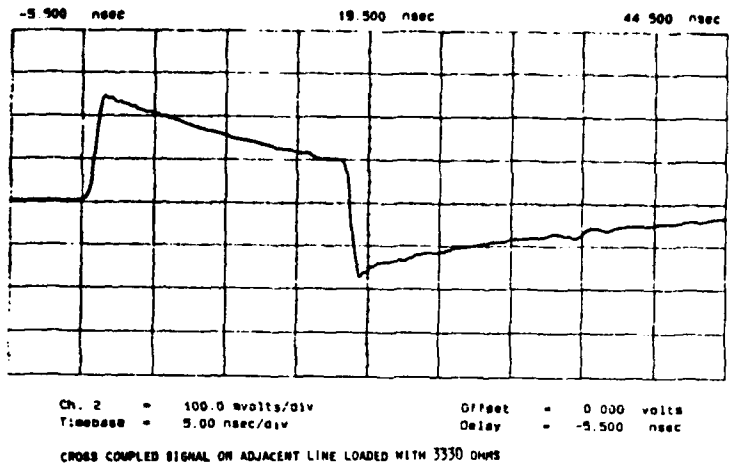


Figure 7.5(a) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.344 Cavity).



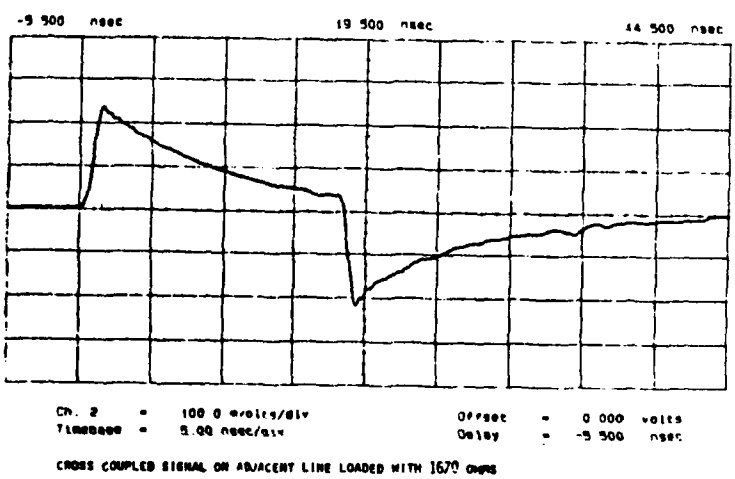
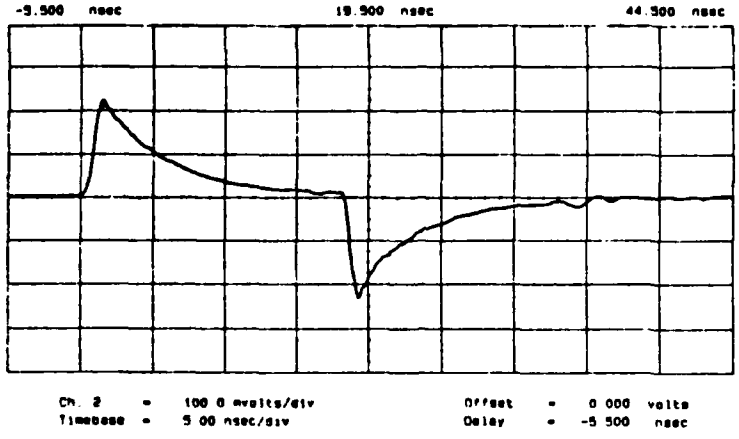


Figure 7.5(b) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.344 Cavity).



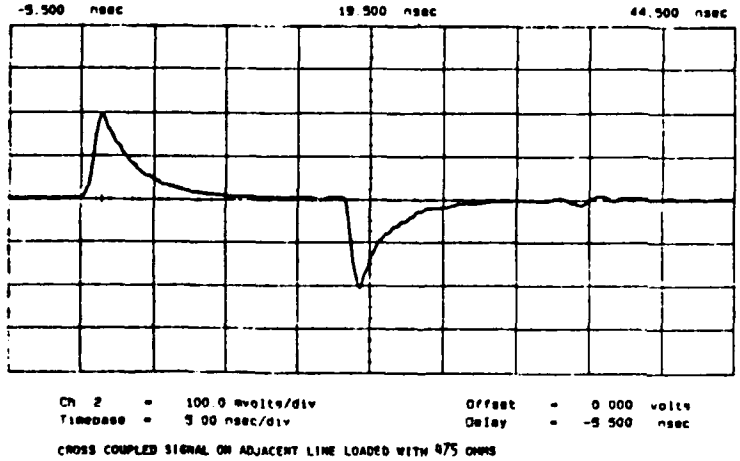


Figure 7.5(c) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.344 Cavity).

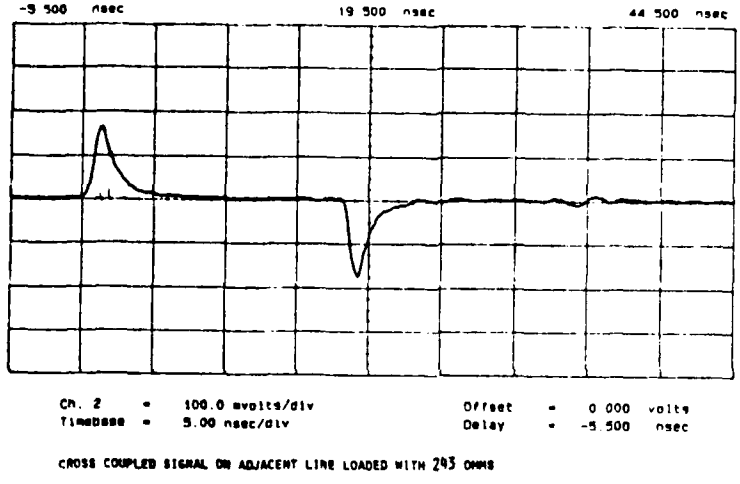


Figure 7.5(d) - Crosstalk As a Function of Load Resistance for 64 I/O Leadless Chip Carrier (0.344 Cavity).

The accuracy of this measurement can be enhanced by increasing the load resistance and the pulse width to increase the charge time to a value more easily observed.

The effective coupling capacitance can be used to calculate the approximate level and wave shape of the crosstalk waveforms. This information is important because both the level and the pulse width of the crosstalk must be known to predict if the coupled pulse can be sensed by a susceptible, adjacent receiver pin. For example, if the effective coupling capacitance is very small, only a very narrow "spike" can be coupled to an adjacent receiver. If the spike is much narrower than the minimum detectable pulse width for the target logic family, or if its level is well below the "1" threshold, the coupled energy cannot contribute significantly to circuit performance degradation. As crosstalk pulse widths increase towards the minimum pulse width of the target logic family, the potential for circuit problems due to noise or time "jitter" increases. For very large values of effective coupling capacitance, the pulse width and height of the crosstalk could be large enough to cause the susceptible receiver to toggle. The probability of this happening in an actual circuit environment becomes larger as the maximum operating frequency of VHSIC devices increases, and the physical characteristics of the packaging (closer spacings, longer runs) create higher coupling capacitances.

There are three ways to use the pulse measurement technique in the evaluation of the crosstalk potential of VHSIC packages:

- As a relative comparison of readings from one package type to another or for finding the best or worst case runs within a given package, a simple comparison of coupling capacitance (C_C) values is adequate.

- Values of coupling capacitance (C_C) determined by the general method described above can be applied to models in a pulse-response type of circuit simulator such as SPICE 2 to calculate crosstalk levels and pulse-widths for various values of IC drive/load impedance and for various values of pulse rise times.

- Direct readings of crosstalk can be taken by simulating the circuit impedance and rise times in the test setup with appropriate pulse generators and load resistors/capacitors. Actual IC's can also be used, if practical, to generate the pulses and provide actual receiver loads.

CONCLUSIONS

Measurement of effective coupling capacitance between signal runs in a package using the pulse measurement technique has proven to be a simple and effective means of evaluating the relative readings of crosstalk between

packages. The technique can also predict crosstalk for various impedance values from data taken with a single resistor load value. Circuit simulations using the measured effective capacitance values yield crosstalk predictions of the approximate shape and level of the actual crosstalk pulses observed.

A MIL-STD-883 test method based on this procedure would yield reliable comparison data on a package's susceptibility to crosstalk. The relative simplicity of the measurement and test equipment requirements make this a practical technique.

RECOMMENDATION

- Include the Crosstalk Measurements for Digital Microelectronic Device Packages method in MIL-STD-883 to evaluate packages for potential problems with crosstalk.

TASK 8: GROUND IMPEDANCE

OBJECTIVE

The purpose of this task is to develop a measurement technique to measure the time variant voltage differential between the package ground and the system ground. High voltage differentials will lead to reduced noise immunity of the logic devices. The same problem can occur in the package's power supply circuit.

METHODS:

As frequencies increase, the current paths to the ground return become more critical. The ideal situation would be to provide a massive ground or ground plane and power plane. These planes should be an integral part of any high frequency package. In many multi-pin packages, the internal ground and power connections are attached to the system through wire bonds and relatively long high impedance runs. Problems occur when ground and power currents must travel an appreciable part of a wavelength. This becomes more of a problem at higher frequencies, since wavelengths are shorter. In high speed digital circuits, the fast leading and trailing edges of the pulses are rich in high frequency harmonics. The result is that the logic device is attempting to force high-level, high-frequency currents in a series-inductive circuit (the ground). Narrow voltage spikes which, in some types of logic circuits are large enough to cause erroneous or false triggering, appear on the DC ground circuit.

Three methods of measuring ground impedance were tried. The first method was differential voltage probing of current pulses. To accomplish this, the package was mounted on a PWB ground plane and the pulse was applied to the package ground. The package ground was connected to the PWB ground plane through wire bonds and a terminating resistor. The measurements were made at the pulse input to the package ground and at the package output pin. The measurements proved to be unstable and could not be repeated, so the technique was abandoned.

The second method attempted was time domain reflectrometry (TDR). The package was mounted on a ground plane and the package ground connected to the PWB ground plane through wire bonds and the package pins. The TDR pulse was applied to the package ground and the reflections observed on the oscilloscope. The setup is difficult to adapt to this application since the TDR is a 50-ohm system and a considerable amount of error is introduced by the test setup. Again reliable data could not be obtained.

The third method employed a Multi-Frequency LCR Meter. Ground impedance becomes a problem when it becomes inductive or resistive. The LCR meter measures inductance and series resistance. It can be used with micro manipulator probes. The most difficult part of the fixturing was probing package contacts at various angles and directions. This was accomplished using micro-manipulators on jacks while holding the package in a vise.

The LCR meter yielded data that was repeatable and relatively easy to acquire. The results clearly separate the relative performances of the various package styles.

The HP4275A Multi-Frequency LCR meter is capable of measuring over the 10 KHz to 10 MHz frequency range. Experience has shown that measurements should only be made at the lowest frequency that gives an on-scale reading. Series inductance readings on circuits with significant stray capacitance pick up errors that get larger as the frequency increases. Referring to Table 8.1,the L data for all package styles shows a decrease with increasing frequency. The 84 I/O pin grid array in particular shows a large decrease in L. The data at the higher frequencies is not reliable. The meter's high frequency capability should only be used for very small inductance values. To reduce the effects of stray capacitance on the inductance readings, the measurement should be performed with the package mounted on an insulating surface so that the package ground plane does not form a capacitive circuit with the LCR meter's ground.

The HP4275A LCR meter also gives a reading of equivalent series resistance (ESR) which is an AC measurement of the resistive component of the ground circuit. This reading may be significant for circuits with very low inductance but for the packages tested, ESR was much smaller than the inductive reactance at VLSI/VHSIC operating frequencies and can be disregarded.

Measurement of ground impedance must include the chip-to-package interconnect media (wire bonds, tape etc.) since these contribute significantly to series L and R values. Using a micromanipulator probe with the LCR meter enables this to be done without difficulty.

The values of inductance measured were small, in the 5 to 20 nH range. 5 nH at 10 KHz has a reactance of 0.314 milliohms, 20 nH at 10 KHz has a reactance of 1.257 milliohms. Neither of these values of reactance would cause any problem, but a transition which had no frequency components above 10 KHz would have a rise time of 100 microseconds or greater, too slow to be of interest. A pulse with a risetime in the 10 nanosecond range has primary frequency components up to 100 MHz. At 100 MHz,5 nH has a reactance of 3.14 ohms and 20 nH has a reactance of 12.57 ohms. This is a significant amount of reactance and the risetimes are still not in the range of present high speed logic. Consider a pulse with a risetime of 1 nanosecond. It has

primary frequency components of 1 GHz. At 1 GHz, 5 nH has a reactance of 31.4 ohms and 20 nH has a reactance of 125.7 ohms. These values of reactance are large enough for a 10 mA current to cause a voltage spike of 1 Volt. Risetimes faster than 1 nanosecond are common and will need packages which have much less inductive reactance to be useful. The limits will have to be set by the user because they are dependent not only on the type of logic but also the application.

Calculation of the level of common-mode ground noise for a particular IC application requires knowledge or measurement of the value of maximum current step (I_Δ) that can be expected and the typical rise/fall times (T_t) associated with this current pulse. The rise/fall times will typically be longer than the transition times for a single drive pin because all pins cannot switch at precisely the same time. Applying the maximum current step values in the series ground reactance value at the frequency of the primary harmonic of the current stage yields an approximation of the peak noise spike value:

$$X = X_L + R$$

where $X_L = 2\pi fL$

R = ESR reading from LCR meter

L = L reading from LCR meter

$$f = \frac{1}{T_t} .$$

Therefore the peak voltage spike value will be approximately equal to $I_\Delta \bullet X$.

RESULTS

The data for the five packages measured is in Table 8.1.

CONCLUSIONS

The above measurement technique is a good method of determining if a grounding strategy is adequate for a particular logic family. The technique is easy to implement and, coupled with some simple calculations, meaningful decisions can be made. The readings are made at low frequencies, using one piece of test equipment. No elaborate fixturing is required and the measurements are not difficult to make.

TABLE 8.1 - MEASUREMENT OF GROUND IMPEDANCE
Using the HP4275A Multi-Frequency LCR Meter

Frequency (KHz)	124 I/O Pin Grid Array		64 I/O Leadless CC .375 Cavity		64 I/O Leadless CC .344 Cavity		84 I/O Pin Grid Array		180 I/O Pad Grid Array	
	L	ESR	L	ESR	L	ESR	L	ESR	L	ESR
10	28	674.9	10	333.4	15	367.8	9	123.7	25	278
20	29	674.6	10	333.4	15	367.2	8	123.3	24	237.7
40	28	674.6	10	333.6	14	367	7	124	23	237.7
100	28	675	10	334	14	367	6	125	22	238
200	28	675	10	334	14	366	4	126	21	238
400	28	675	10	334	14	367	3	127	21	239
1000	27	680	9	330	14	370	2	130	20	240
2000	27	680	9	340	13	370	2	130	20	240
4000	27	700	9	350	13	390	1	130	19	270
10000	27	MEASUREMENTS NOT POSSIBLE AT THIS FREQUENCY								

L IN NANOHENRIES ESR IN MILLIOHMS

RECOMMENDATIONS

- Include the Ground and Power Supply Impedance Measurements for Digital Microelectronic Device Packages test method as part of MIL-STD-883.

TASK 9: STATIC DC RESISTANCE

OBJECTIVE

The purpose of this task is to measure the resistance of the package runs. As the package runs become denser they also become narrower, introducing higher resistance. This contributes to signal transmission attenuation.

METHOD

Two methods were used to make measurements on sample packages. The first was a two-probe method, and the second, a four-probe method. In both cases, the intent was to measure the contact resistance and to subtract this value from the total run resistance plus contact resistance measurement.

In the milliohmmeter method, two probes were used, one at each end of the package run to be measured. The contact resistance for the pair was determined by placing the probe tips as closely as possible on the package run. This resistance reading could be attributed to the probes, then subtracted from a total resistance reading between pairs. These measurements were repeated to check on the precision of the technique. The test is shown schematically in Figure 9.1.

For packages with very low DC resistance values, the errors associated with the two-probe method are too high. Therefore, a four-wire method was also used. The principle was to inject a known current through the package run, and measure the voltage drop across the runs. The resistance was calculated using Ohm's Law.

The test set-up is shown in Figure 9.2. Two package pins were wirebonded to the same chip pad. A known current from a precision current source was forced through the pins. A high impedance differential microvoltmeter (an HP419A Differential Null Voltmeter) was used to measure the voltage from the chip pad to the external solder joint. The resistance was calculated using: $R = V/I$.

RESULTS

Results from the milliohmmeter method are given in Table 9.1.

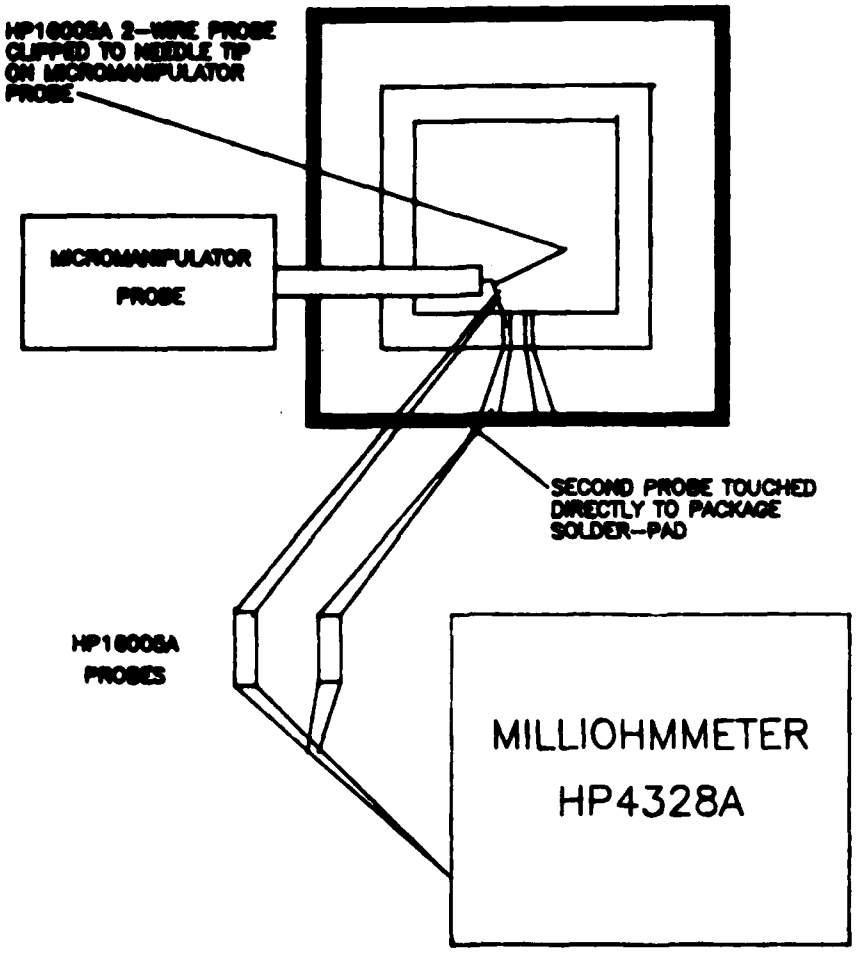


Figure 9.1 - Milliohmmeter Method for Measuring DC Resistance.

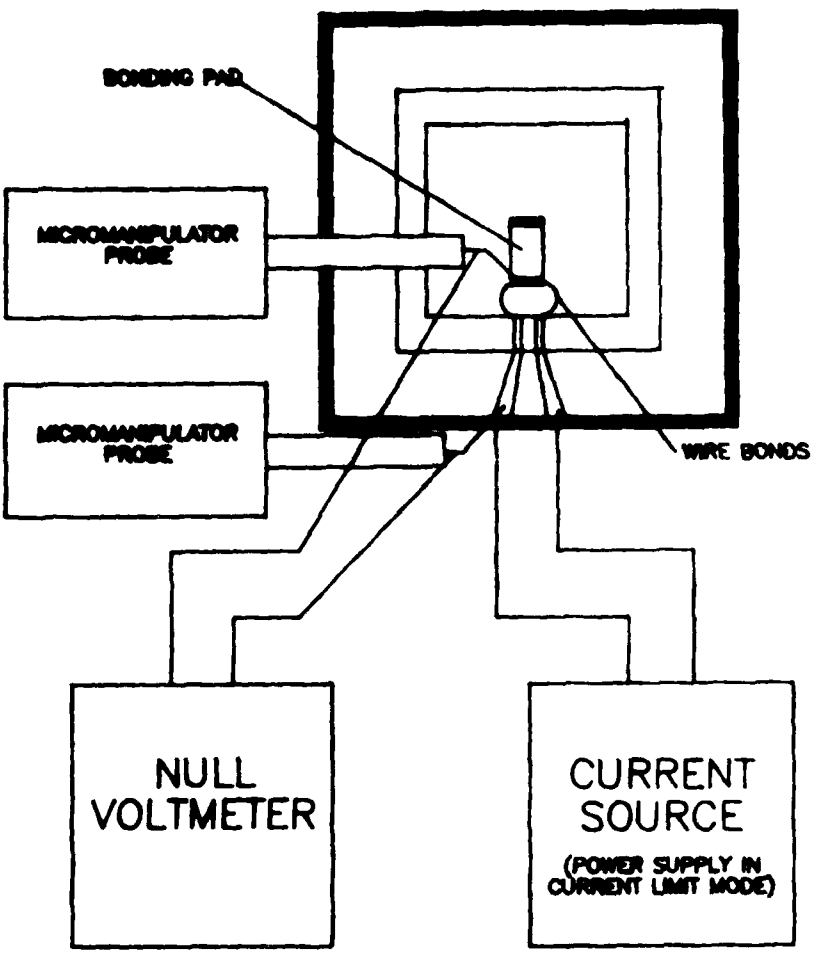


Figure 9.2 - DC Null Voltmeter Method for Measuring DC Resistance.

TABLE 9.1 - DC RESISTANCE

Package Type	Resistance (mΩ)
124 I/O CC	485
64 I/O CC (0.375 Cavity)	325
64 I/O CC (0.344 Cavity)	355
84 I/O CC	345
84 I/O Pin Grid Array	245
180 I/O Pad Grid Array	245

CONCLUSIONS

Measurement of DC Resistance is straightforward but the physically small size of chip-pads and specialized interconnect media such as tape require the use of specialized probe fixtures. By itself, DC Resistance does not warrant an independent MIL-STD-883 Test Method. These techniques can be integrated into other test methods.

RECOMMENDATIONS

- The DC resistance measurement techniques should be used to perform the resistance measurement (Paragraph 3.3) of the proposed Microelectronics Package Digital Signal Transmission test method.

TASK 10: BOND PULL EFFECTIVENESS EVALUATION

OBJECTIVE

To evaluate the impact of finer chip-to-package bond spacing, tape automated bonding, and new package geometries such as double-ledge configurations on the performance of bond pull test methods.

METHOD

Ten wire bond samples were assembled for this evaluation. Five were in double-ledge 180 I/O pin grid array packages, and five in 84/40 leadless chip carriers with a single bonding ledge. The chips were wire bonded to each package type by a Mech-El automated bonding system using 1.25 mil diameter aluminum wire.

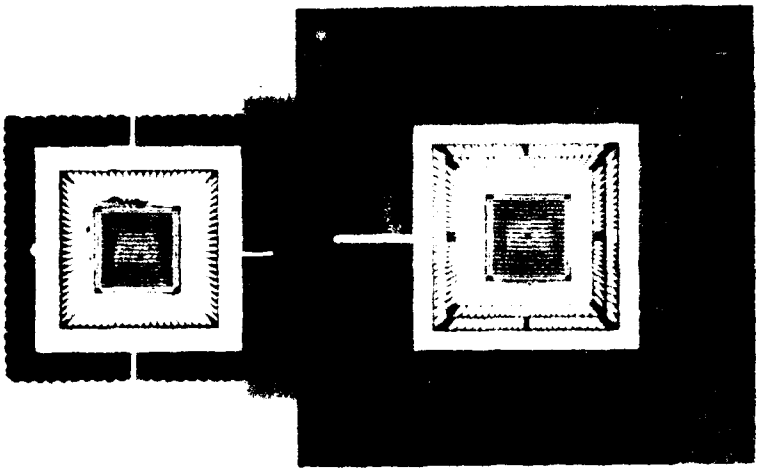
In addition to the wire-bond samples, five tape-automated-bond (TAB) samples, each with 42 leads, were mounted on a metal plate with epoxy. The spacing between leads on these samples varied, but the minimum spacing was 8 mils at the chip and fanned out to 20 mil at the "package". The metallization itself was 3.5 mil wide at the chip and was supported by a polymer film tape. Examples of both wire and TAB samples are shown in Figure 10.1.

The wire bond and TAB connections all were checked for electrical continuity by probing from the chip pad to the package pad. Since resistance readings were highly dependent on the probe pressure, the continuity was checked with a Tektronix Model 576 Curve Tracer. The current-voltage characteristic of each bond was checked with positive and negative voltage and monitored for a change in slope.

Both wire bonds and TAB samples were destructively tested both by pulling and shearing. In both cases, the pull test was performed in accordance with Method 2011, Condition D, by inserting a hook under the wire or lead and pulling to destruction.

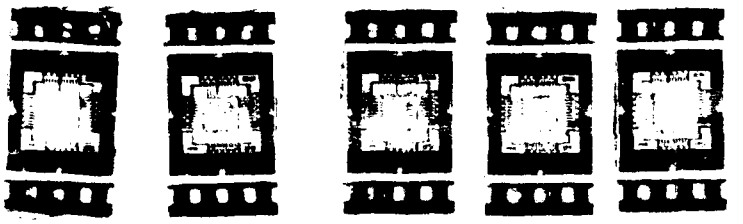
Reports in the literature of a shear test for gold ball bonds[1] motivated applying a similar test to these samples. This proved to be very difficult as the wedge bonds had insufficient height to allow proper alignment of the shear tool. In many cases, the tool either scraped over the top of the bond or pushed into the bond pad. Continued practice by the operator was not able to overcome this problem. Tools used in testing these bonds are shown in Figure 10.2.

1 "Destructive Shear Testing of Ball Bonds"
Charles, Harry K.
The Johns Hopkins University
Applied Physics Laboratory



MAG: 2X

Figure 10.1(a) - Wire bond samples: Single ledge 84/40 leadless chip carrier (left), and double ledge 180 I/O pin grid array package (right).



MAG: 1X

Figure 10.1(b) - TAB samples: 42 leads each, mounted on metal plate with epoxy.

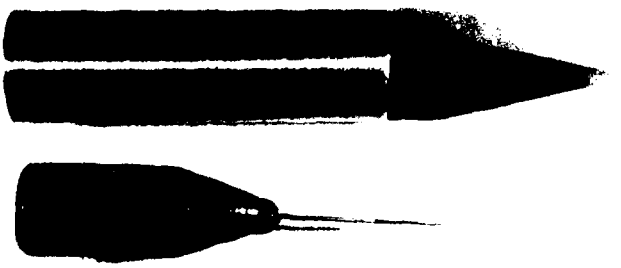


Figure 10.2 - Bond test tools: Shear tool (top), Pull hook (bottom).

The samples were subjected to the test plan shown in Figure 10.3. After initial continuity, pull, and shear tests as described above, the packages were cycled from -55°C to +125°C per MIL-STD-883, Method 1010. Interim tests were performed after 10, 25 and 50 cycles; final tests were performed after 100 cycles. At interim test points, ten wires were pulled and five sheared. In the case of the double-ledge bond configuration, five wires were pulled from the inner ledge and five from the outer ledge.

RESULTS

A sample test data sheet for the pull and shear tests is included as Table 10.1.

The continuity results were the same for all bonds on all packages: no open circuits occurred during environmental stress. Since no electrical failures or degradation were noted during the temperature cycling sequence, the average pull strengths for each of the chip carrier and pin grid array packages were plotted to check for systematic trends. This is shown in Figure 10.4. The post 100-cycle strength averages were lower than the initial averages, but probably do not reflect a statistically significant trend. Greater variation occurred from 10 to 25 cycles where the averages increased. These variations can be explained by use of a different pull test machine after cycles 10, 50 and 100 than for the initial and 25-cycle measurements. Different machines were used when equipment failure prevented testing on a single machine. Both were reported to be in calibration at the time of use, thus, these data may show the expected variation between testers.

A total of 754 wires were pulled. The mean pull strength was 7.9 g-force, with a standard deviation of 1.4. The mean minus three sigma lower limit was then 3.7 g-force. This appears to support the 3.0 g-force minimum strength requirement of Method 2011 for 1.25 mil diameter aluminum wire (all test data were above this limit). Since these bonds maintained continuity throughout environmental stress, the pull results agreed with the physical reality, i.e., all the bonds were of adequate quality.

The averages of shear strengths for wire bonds on both package types are shown in Table 10.2. The standard deviations for these measurements were, in general, a higher percentage of the average reading indicating a wide spread of data. This is shown graphically as a frequency distribution in Figure 10.5. The difficulty in performing this test apparently led to poor repeatability in the results.

The average pull test data for TAB samples is plotted as a function of completed temperature cycles in Figure 10.6. Again, it shows no clear trend, but a variation due to the tester used. Again the pull strengths passed the MIL-STD-883 limit of 3.0 g-force for 1.25 mil wires. The metallization here was not a 1.25 mil diameter round wire, however, but a rectangular shape

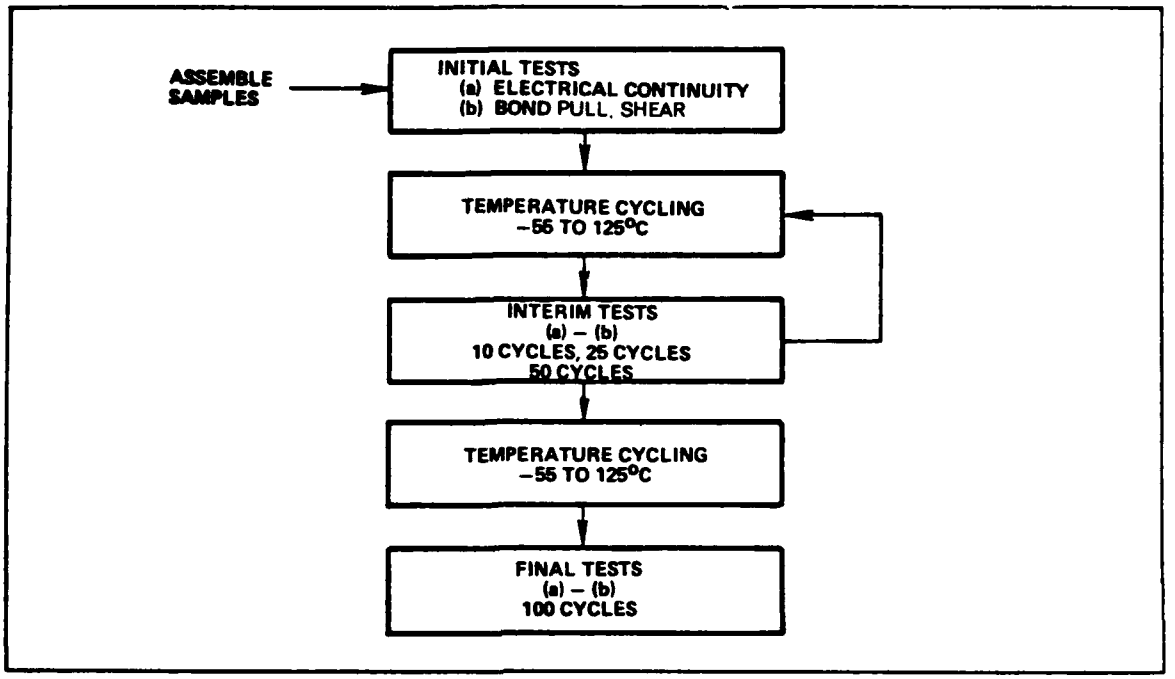


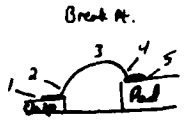
Figure 10.3 - Test plan for bond pull and bond shear samples.

TABLE 10.1 - CC POST 50 CYCLES PULL/SHEAR DATA

DATA RECORDED AT PAEL — Pull/Shear Test (G.F.)

DEVICE TYPE: HCC
MANUFACTURER:
QUANTITY: 5
REMARKS:

PROGRAM: V/V PID
DSO NUMBER:
TASK NUMBER:
DATE: 1/30/85
SIGNATURE: TR



TEST CONDITIONS:

TEST EQUIPMENT:

DATA SHEET OF

SPECIMEN NO.	1	B.P.	2	B.P.	5	B.P.	6	B.P.	9	B.P.
Bond #46	6.5	2	7.9	2	6.5	2	7.9	2	4.8	2
47	7.9	2	8.1	2	7.7	2	8.5	2	8.1	2
48	7.8	2	7.6	2	6.2	2	7.3	2	6.6	2
49	8.2	2	9.6	2	7.2	2	8.3	2	7.6	4
50	9.3	2	8.4	2	6.8	2	8.1	2	6.8	2
51	9.2	2	8.5	2	6.9	2	6.6	2	6.6	2
52	8.9	2	6.9	2	8.1	2	7.4	2	8.3	2
53	9.2	2	8.6	2	7.5	2	8.5	2	7.4	2
54	9.0	2	8.3	2	7.7	2	8.8	2	6.8	2
55	9.7	2	9.3	2	8.2	2	7.4	2	7.8	2
$\bar{x}$	8.6		8.3		7.3		7.9		7.0	
σ	1.0		0.8		0.7		0.7		1.0	
Shear 56	25		36		3		15		32	
57	38		24		6		25		25	
58	11		27		45		5		4	
59	12		31		38		17		10	
60	4		19		42		26		11	
$\bar{x}$	18.0		27.4		26.8		17.6		16.4	
σ	13.5		6.5		20.5		8.5		11.6	

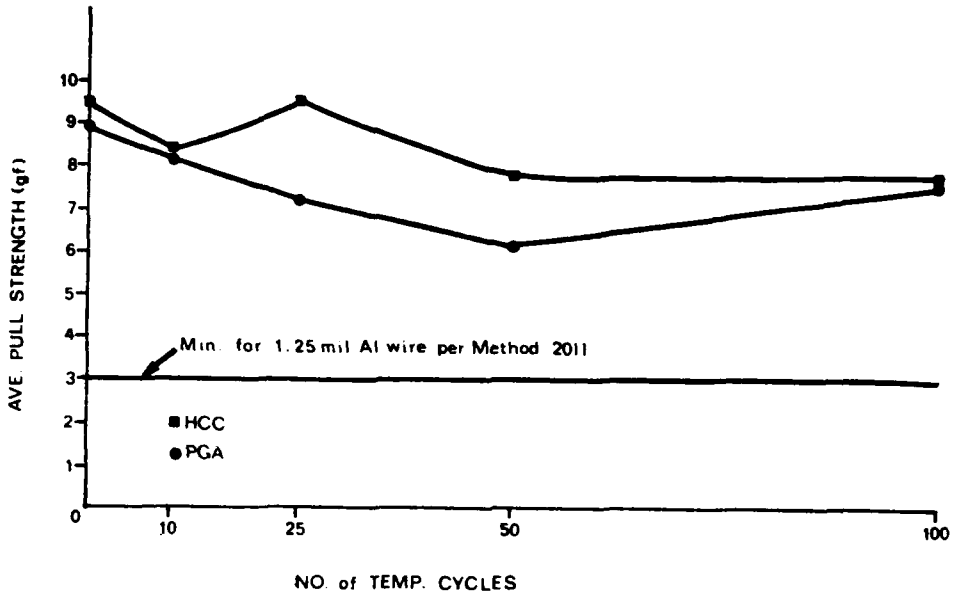


Figure 10.4 - Average Pull Strength Versus No. of Temp. Cycles for CC's, and Pin Grid Arrays.

TABLE 10.2 - AVERAGE WIRE BOND SHEAR STRENGTHS

Test Point (No. of Temp. Cycles)	Average Wire Bond Shear Strengths (g-force)					
	N	CC	N	PGA	N	Combined
0	25	15.0	25	16.8	50	15.9
10	25	19.3	25	25.4	50	22.4
25	25	26.3	25	26.6	50	26.5
50	25	21.2	25	23. 7	50	22.5
100	25	18.4	25	20.5	50	19.5
Total all Tests					250	21.4 σ=13.9

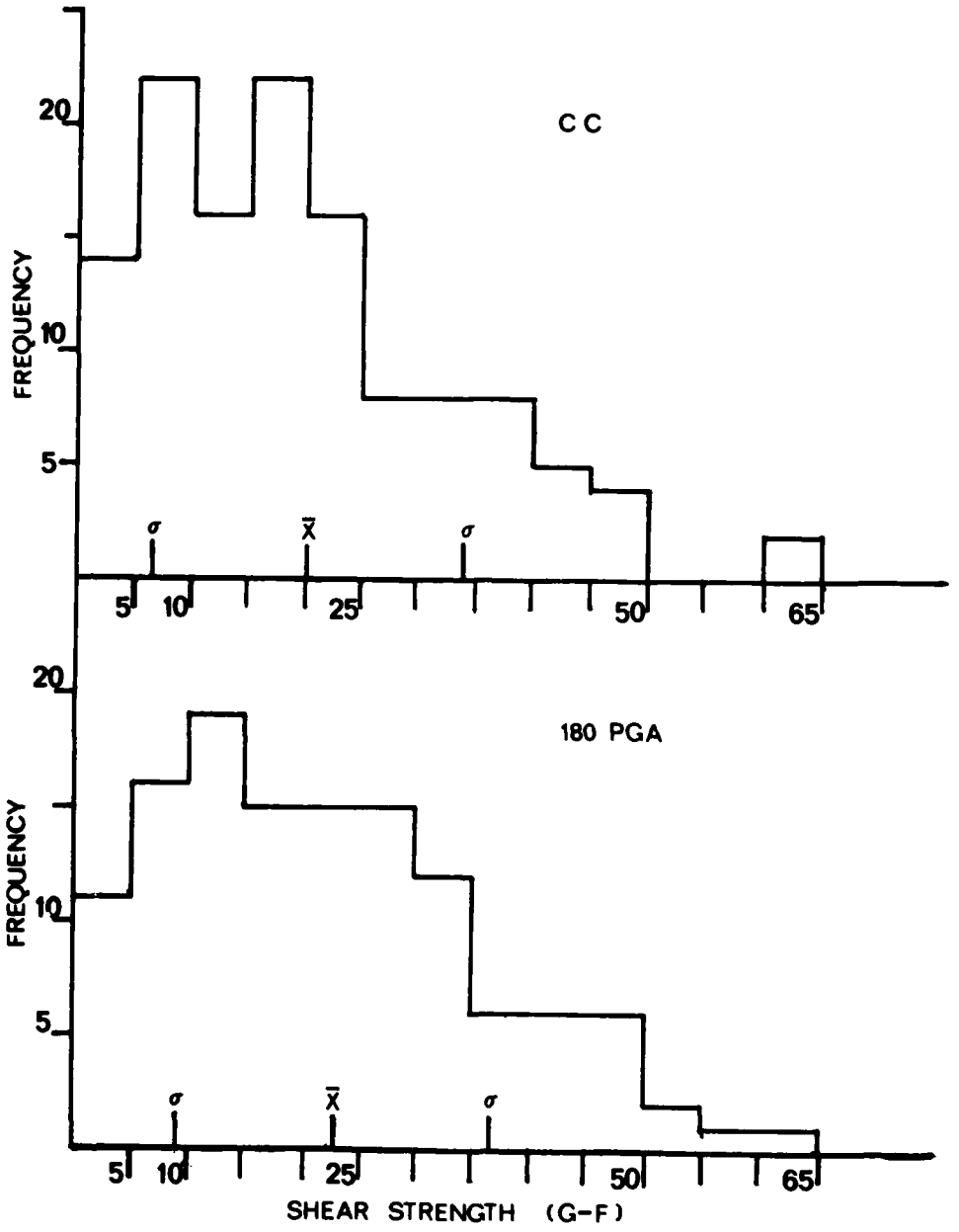


Figure 10.5 - Histogram of Wire Shear Results.

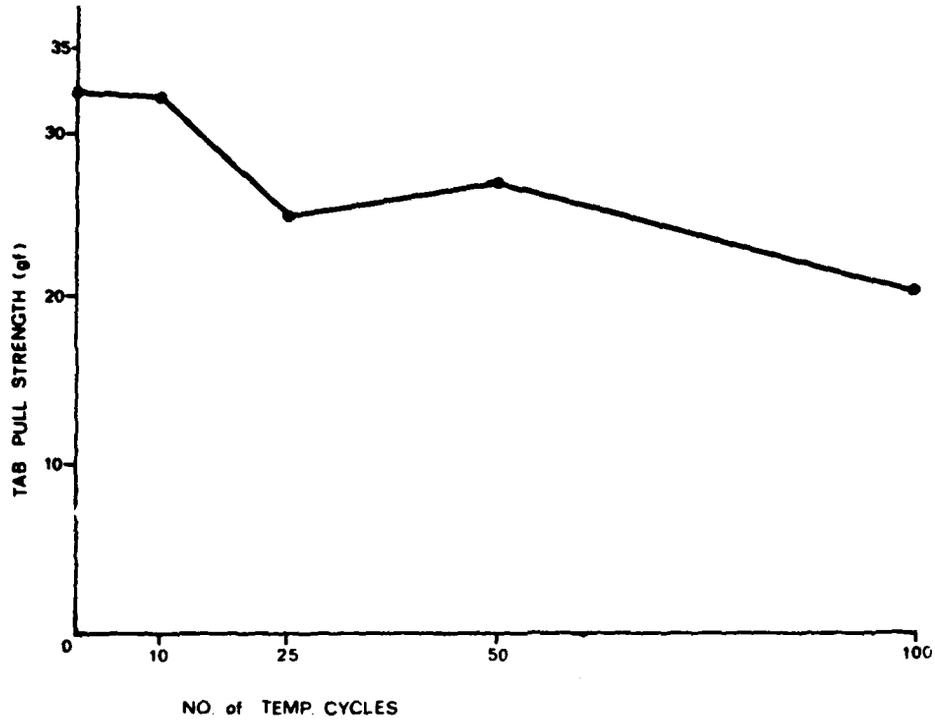


Figure 10.6 - TAB Pull Strength Versus No. of Temp. Cycles.

measuring 3.5 mil width, and roughly 0.7 mil in thickness. The cross-sectional area was 2.5×10^{-6} $in.^2$, or the equivalent of a wire bond 0.9 mil in diameter. The strength for a bond this size would be roughly 2.1 g-force. The pull strengths far exceeded this limit.

Frequency distributions for the pull and shear strengths of TAB samples are shown in Figure 10.7. As with the wire bond samples, the shear data has a more widespread distribution, which is not well centered about the mean.

CONCLUSIONS

The pull test for bond strength performed to Method 2011, Condition D, was a valid test for the aluminum wire bond samples. The test also provided repeatable results for TAB samples and can be applied to this type of interconnection where testing in this manner is possible. A standard for tape bonds based on cross-sectional area relative to that of an equivalent aluminum wire bond would be reasonable.

Shear testing of either aluminum wire bonds or tape bonds was difficult to perform, and led to no significant results.

Although pull testing was possible on the TAB samples assembled for this study, it may not be possible for very sophisticated TAB designs. Attempts to pull test 2.5 mil leads on a TAB sample provided by Honeywell were fruitless. Shear testing of these bonds also proved impossible. More study for methods to test these types of bonds will be required. One potential method touched on briefly here was ultrasonic imaging of tape bonds. Since ultrasonic images are sensitive to the connection between the chip and the tape, the method should theoretically provide information about the bond quality. Images of a TAB sample from Sonoscan's laser acoustic microscope are shown in Figure 10.8. This is a promising method, but requires more study before it can be incorporated in MIL-STD-883.

RECOMMENDATIONS

- Perform pull tests per Method 2011, Condition D for aluminum wire bonds as written.
- Pull testing for tape-automated-bond (TAB) samples can be performed on some samples. In this case, a minimum strength based on cross-sectional area equivalent wire bond should be required.
- Pull testing may not be possible on some of the more finely spaced TAB samples. Use of an alternative method should be investigated.
- Shear testing should not be applied to wedge bonds or tape bonds.

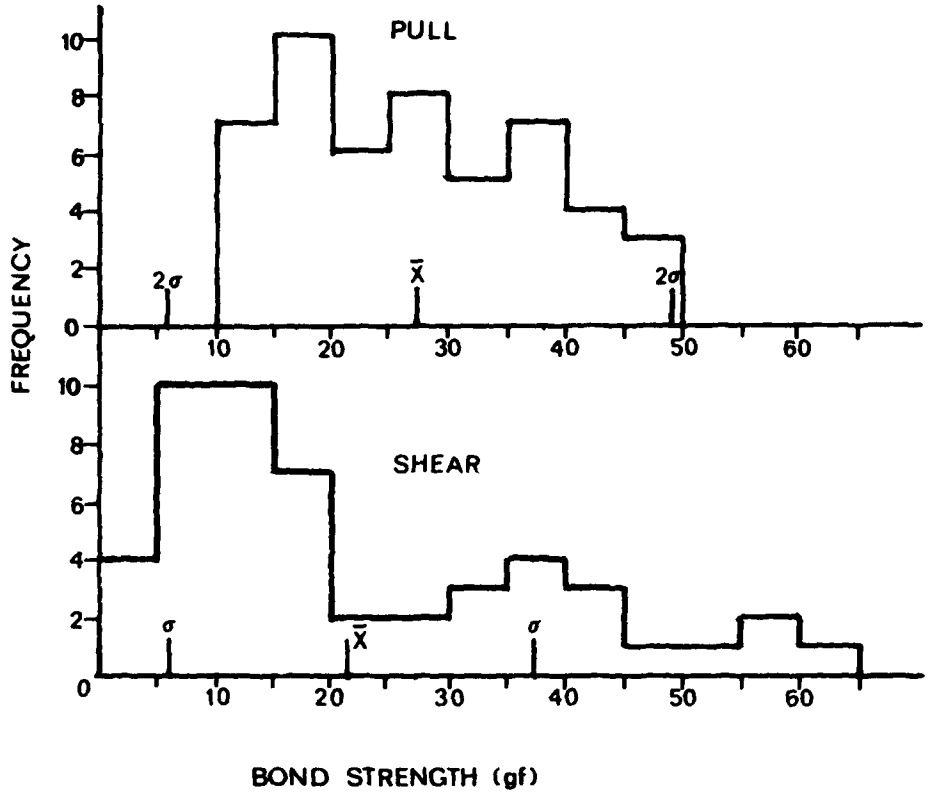


Figure 10.7 - Frequency Distributions of TAB pull and shear strengths.

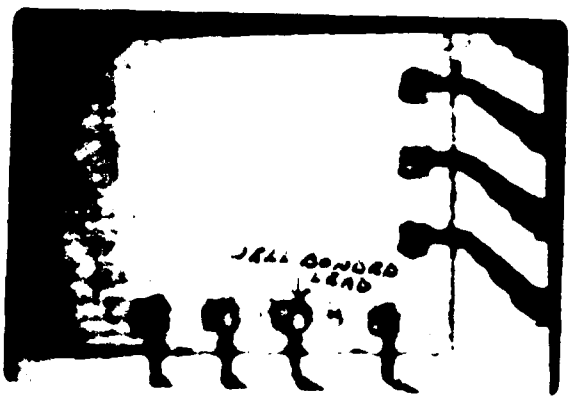


Figure 10.8 - Ultrasonic image of TAB sample (produced by Sonoscan).

TASK 11: PEEL TEST EVALUATION

OBJECTIVE

To evaluate the effectiveness of a bond peel test rather than a pull test on tape-automated-bonding (TAB) samples.

METHOD

Five TAB samples were assembled for this evaluation. The samples each had 42 leads, and were epoxy bonded to a metal plate. The same samples were used in Task 10, and are shown in Figure 10.1(b).

The leads themselves were gold-plated copper metallization on a polymer film. Near the chip pads the metallization was 3.5 mil in width and near the package end 20 mil in width. At the chip, the traces were 2.5×10^{-6} $in.^2$ in cross-sectional area.

The peel test itself was performed similarly to pull testing, but using a tweezer attachment to grip the TAB lead. The tweezer is shown in Figure 11.1. The film between the leads was cut with a scalpel before testing. Peel testing was performed on a Dage Model MCT-15 Microbond Tester.

The test samples were subjected to the test plan shown in Figure 11.2. This was identical to that of the Pull Test Evaluation in Task 10; the parts tested were used for both evaluations. Electrical continuity of the bonds was measured by probing from the chip pad to the package pad. A Tektronix model 576 Curve Tracer was used to check the current-voltage characteristic for each connection. The samples were cycled from -55°C to +125°C per MIL-STD-883, Method 1010 for a total of 100 cycles, with interim tests after 10, 25 and 50 cycles.

RESULTS

The data sheet for the bond peel measurements as well as the pull and shear data that were part of Task 10 is shown in Figure 11.3. The electrical continuity of each bond was maintained throughout the environmental stress sequence; there were no failures.

Figure 11.4 shows a plot of peel strength versus number of temperature cycles for the five samples. Each point is the average of the two bonds that were peeled on the sample. There were no trends in bond strength noted as a function of temperature stress. The averages were spread between values of 16 grams-force and 47 grams-force.

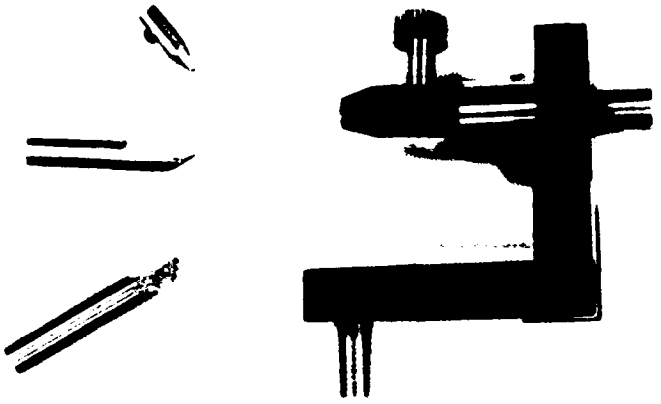


Figure 11.1 - Tweezer used for TAB peel test.

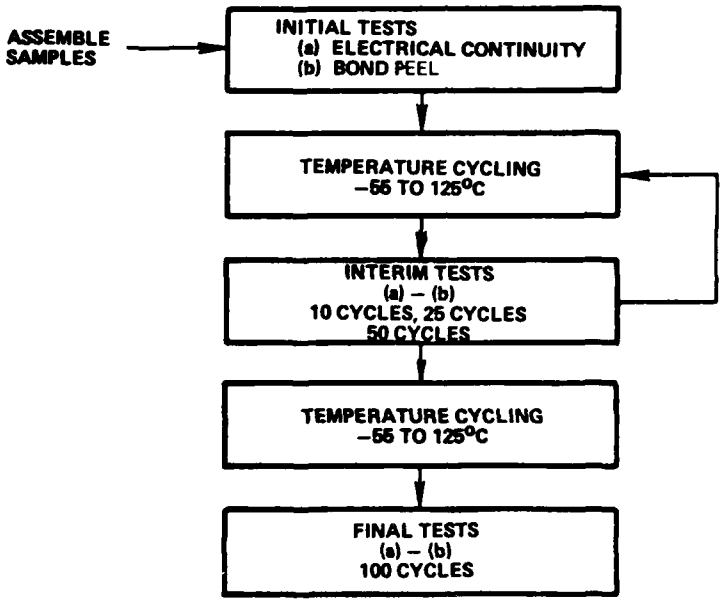
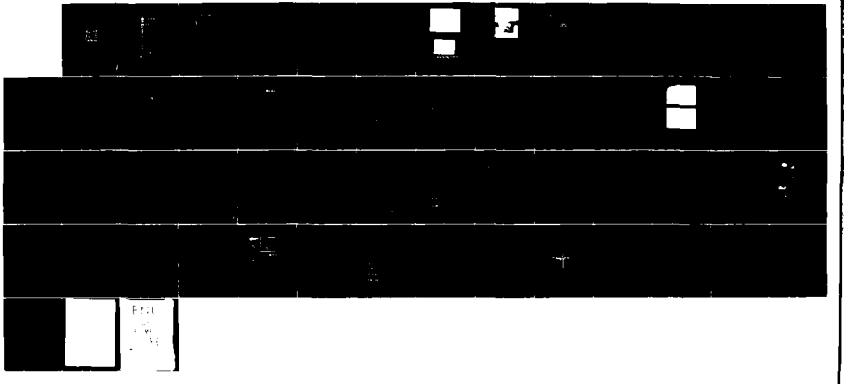
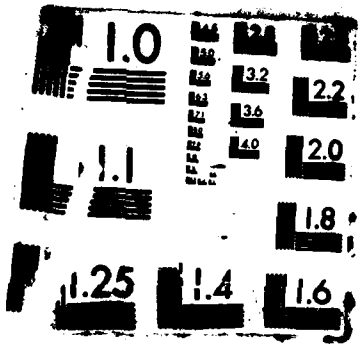


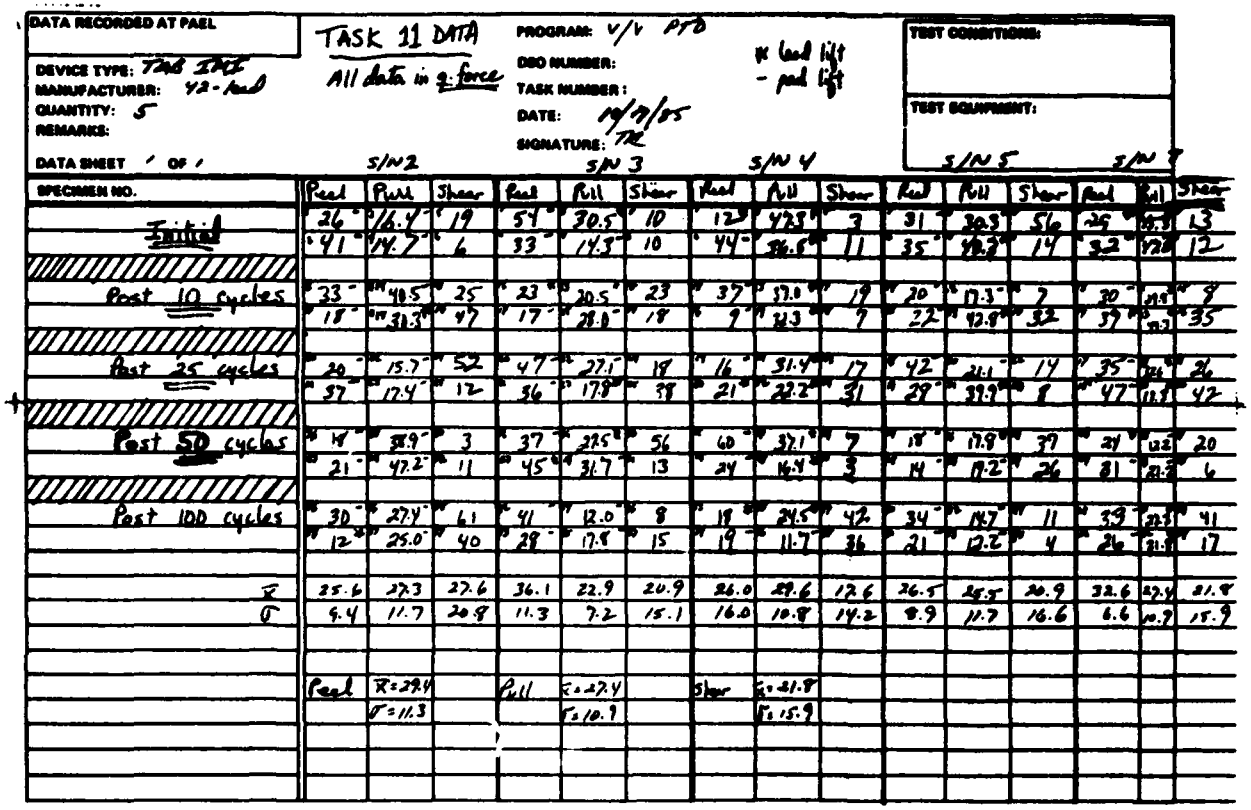
Figure 11.2 - TAB peel test plan.

AD-A182 360 VLSI/VHSIC (VERY LARGE SCALE INTEGRATED/VERY HIGH SPEED INTEGRATED CIRCUI..(U) RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV K E CLARK DEC 86 RADC-TR-86-94 3/3

UNCLASSIFIED F30602-84-C-0015 F/G 9/1 NL




1.0
3.2
2.2
3.6
4.0
2.0
1.1
1.8
1.25
1.4
1.6



DATA RECORDED AT PAEL

DEVICE TYPE: TAB IPAT
MANUFACTURER: Y2-Aerol
QUANTITY: 5
REMARKS:

DATA SHEET 1 OF 1

TASK 11 DATA
All data in g-force

PROGRAM: V/V PTD
DBO NUMBER:
TASK NUMBER:
DATE: 10/7/85
SIGNATURE: TR

* load lift
- pad lift

TEST CONDITIONS:

TEST EQUIPMENT:

SPECIMEN NO.	S/N 2 Peel	S/N 2 Pull	S/N 2 Shear	S/N 3 Peel	S/N 3 Pull	S/N 3 Shear	S/N 4 Peel	S/N 4 Pull	S/N 4 Shear	S/N 5 Peel	S/N 5 Pull	S/N 5 Shear	S/N 7 Peel	S/N 7 Pull	S/N 7 Shear
Initial	26	16.4	19	54	30.5	10	12	42.5	3	31	30.3	56	25	15.9	43
	41	14.7	6	33	14.5	10	44	36.6	11	35	49.2	14	32	17.8	12
Post 10 cycles	33	40.5	25	23	20.5	23	37	37.0	19	20	17.3	7	30	19.9	8
	18	31.3	47	17	28.0	18	9	42.3	7	22	42.8	32	39	20.2	35
Post 25 cycles	20	15.7	52	47	27.1	18	16	31.4	17	42	24.1	14	35	14	26
	37	12.4	12	36	17.8	38	21	22.2	31	29	39.9	8	47	11.8	42
Post 50 cycles	14	38.9	3	37	22.5	56	60	32.1	7	18	17.8	39	24	12.8	20
	21	47.2	11	45	31.7	13	24	14.4	3	14	11.2	26	31	21.2	6
Post 100 cycles	30	27.4	61	41	12.0	8	18	24.5	42	34	14.7	11	39	23.3	41
	12	25.0	40	28	17.8	15	19	11.7	36	21	12.2	4	26	21.8	17
$\bar{x}$	25.6	27.3	27.6	36.1	22.9	20.9	26.0	29.6	17.6	26.5	25.5	20.9	32.6	22.4	21.8
σ	9.4	11.7	20.8	11.3	7.2	15.1	16.0	10.8	14.2	8.9	11.7	16.6	6.6	10.7	15.9
	Peel $\bar{x}$=29.4 σ=11.3			Pull $\bar{x}$=22.4 σ=10.9			Shear $\bar{x}$=21.8 σ=15.9								

Figure 11.3 - TAB Test Data.

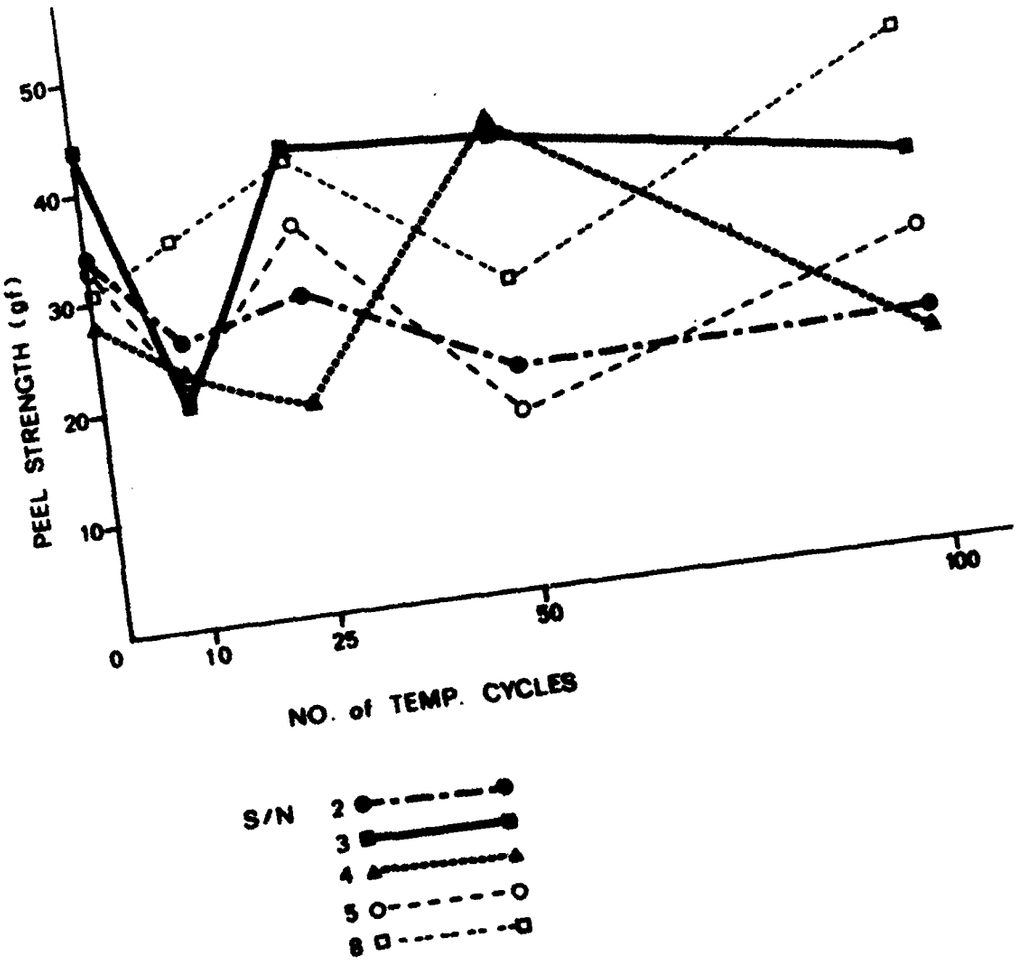


Figure 11.4 - TAR Peel Strength (g-force) Versus No. of Temp. Cycles for each TAR Sample.

The cross-sectional area of the TAB leads was 2.5×10^{-6} in.^{2}. The equivalent bond wire would be 0.9 mil in diameter with a minimum required strength of 2.1 g-force. All bonds exceeded this limit in peel strength.

A frequency histogram for the peel strengths and pull strengths of the TAB samples is shown in Figure 11.5. The average pull strength was 27 g-force, and average peel strength was 29 g-force. A statistical test showed that the two distributions could be considered the same with a 95 percent confidence level.

CONCLUSIONS

Any changes in the bond quality during temperature-cycling were too small to be identified with the peel test technique. All the bonds were of good quality electrically before and after temperature cycling which implies that the peel test measurements should be typical of good quality bonds. The measured strengths were all in excess of 2.0 g-force which would be the limit from Method 2011 for an aluminum wire bond of the same cross-sectional area.

The peel strength results correlated with the pull strength results from Task 10. For these samples the two methods were equivalent.

Performing the peel test was possible on these samples in part from the relatively large spacing of the leads. The film between the leads was cut to enable peeling; this was not possible on samples sent by Honeywell that had only 2.5 mil spacing between leads.

The peel test was only applicable to samples where the geometry allowed easy separation of the leads. On these samples, it was the equivalent of the pull test.

RECOMMENDATION

- A peel test can be interchanged for a pull test where sample geometry makes peel testing easier to perform. The same test limit should be used for either test: comparison to the required minimum pull strength of an aluminum bond wire of equivalent cross-section.

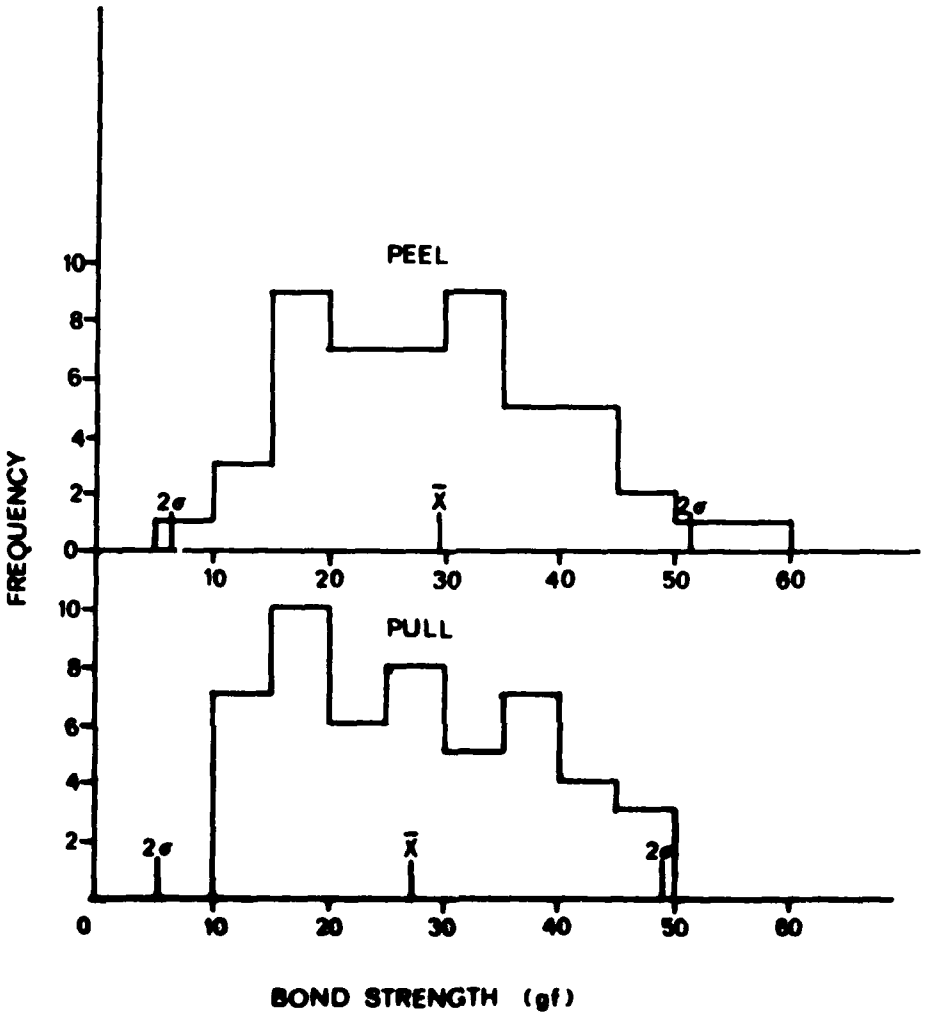


Figure 11.5 - Frequency Distribution of TAB Peel and Pull Tests.

TASK 12: FLIP-CHIP PULL TEST EVALUATION

OBJECTIVE

To investigate the effectiveness of a pull test in assessing the integrity of flip-chip interconnections.

METHOD

The samples were bipolar logic arrays supplied by Cherry Semiconductor of East Greenwich, Rhode Island. The chips were mounted by reflow soldering ceramic substrates metallized with a gold-platinum-nickel paste in the pattern shown in Figure 12.1. The bumped chips were attached to the metallization with 10 percent tin/90 percent lead solder.

The flip-chip solder joints were imaged with a Research Devices, Inc. (Model F) infra-red microscope. This technique was not pursued due to the difficulty in interpreting the image. The flip-chip joints were also imaged using a scanning laser acoustic microscope. A photograph of this image in Figure 12.2 shows the inadequate definition provided by this method.

A destructive pull test was developed to evaluate the flip-chip solder joints. A metal pin with diameter slightly less than the width of the chip was bonded to the chip using a cyanoacrylate adhesive (in this case Eastman 910). The metal pin was attached to the die shear tool which was in turn attached to the Dage microtester load arm. This arrangement allowed a degree of self-alignment in testing. The test configuration is shown in Figure 12.3.

During preliminary attempts to establish a test method, six flip-chips were pulled. As a comparison, ten shear tests were performed to Method 2011, Condition F.

Following these preliminary tests, samples were subjected to the environmental stress plan shown in Figure 12.4. The samples were five substrates; each substrate held two flip-chips. Temperature cycling from -55°C to +125°C in accordance with MIL-STD-883, Method 1010 was performed for a total of 100 cycles. All solder joints were checked for electrical continuity by probing to the metallized pad and back of the chip, then mapping the current-voltage characteristic with a Tektronix Model 576 Curve Tracer. One sample was pulled initially, three were pulled at interim test points, and one after the full 100 cycles.

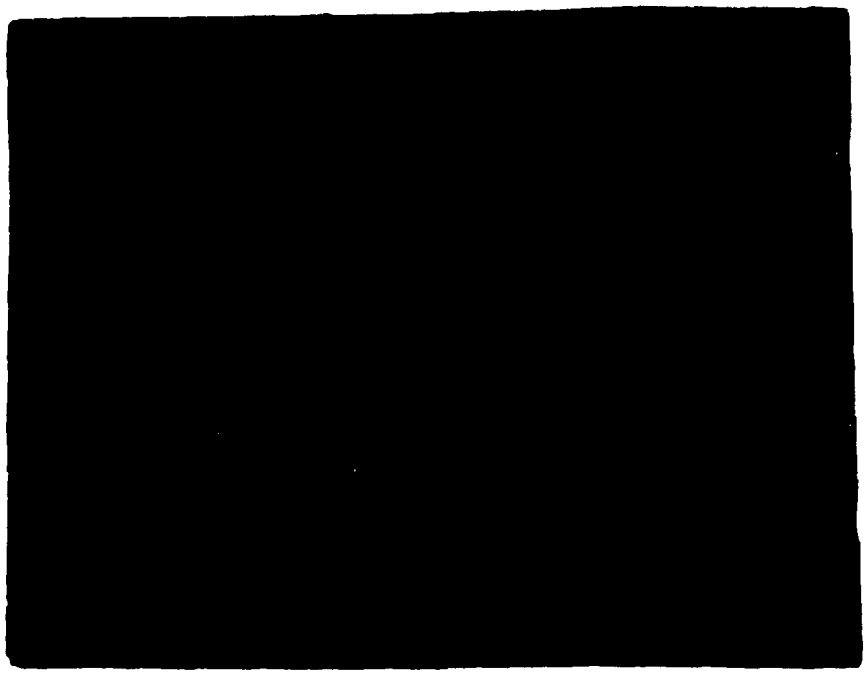


Figure 12.1 - Flip-Chip substrate metallization pattern.

Figure 12.2 - Scanning laser acoustic microscope image of flip-chip sample (produced by Sonoscan).

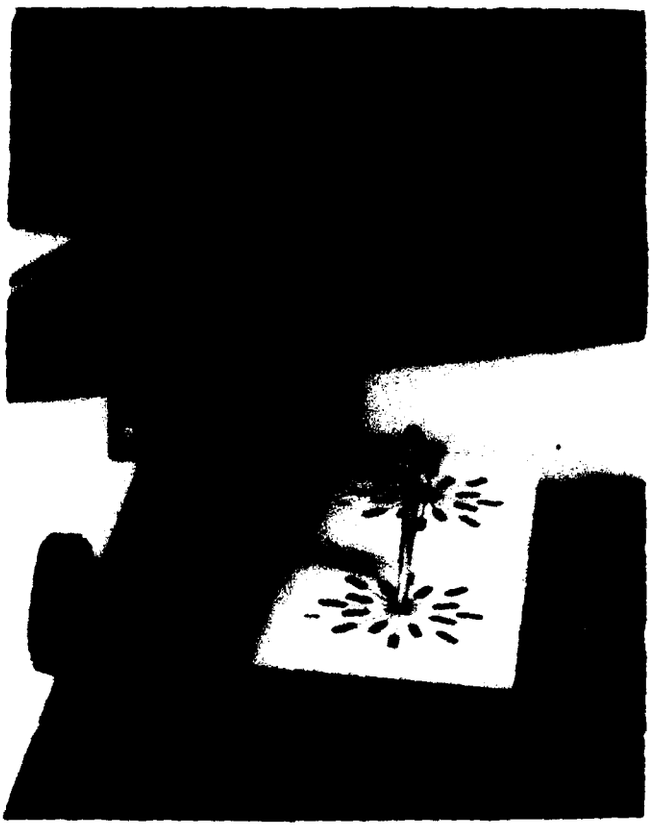


Figure 12.3 - Flip-chip pull test setup.

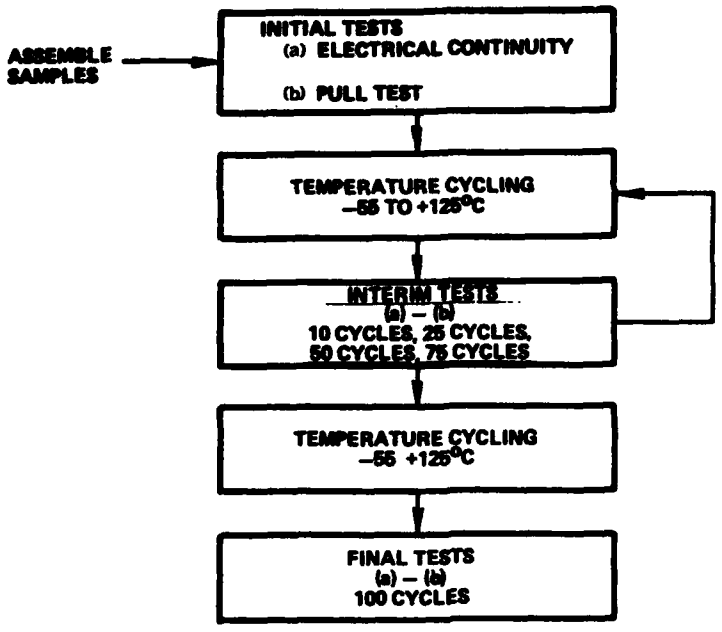


Figure 12.4 - Flip-chip evaluation environmental stress plan.

RESULTS

The pull strengths and shear strengths for the preliminary tests are shown in Table 12.1 below. Note that the average shear strength was 1335 g-force while the Method 2011 Condition F limit for these samples was 80 g-force (16 solder bumps x 5 g-force per bump). The standard deviation for pull testing was about 36 percent of the mean, while the shear test standard deviation was 7 percent of the mean.

TABLE 12.1 - PRELIMINARY PULL AND SHEAR STRENGTHS

Flip-Chip S/N	Pull Test Strength (g-force)
1	4100
2	3150
3	2950
4	3550
5	1700
6	1500
	$\bar{X}$ = 2825
	σ = 1029
	Shear Test Strength (g-force)
7	1300
8	1250
9	1450
10	1500
11	1300
12	1350
13	1350
14	1300
15	1150
16	1400
	$\bar{X}$ = 1335
	σ = 100.1

201

Results of the five pull tests performed during temperature cycling are shown in Table 12.2 below:

TABLE 12.2 - TEMPERATURE CYCLING PULL STRENGTHS

Test Points	Pull Strength (g-force)
Initial	2150
Post 10 Cycle	2100
Post 25 Cycle	3150
Post 50 Cycle	3100
Post 100 Cycle	3900
	$\overline{X}$ = 2890
	σ = 759

Here the standard deviation was 26 percent of the mean. No continuity failures occurred during testing.

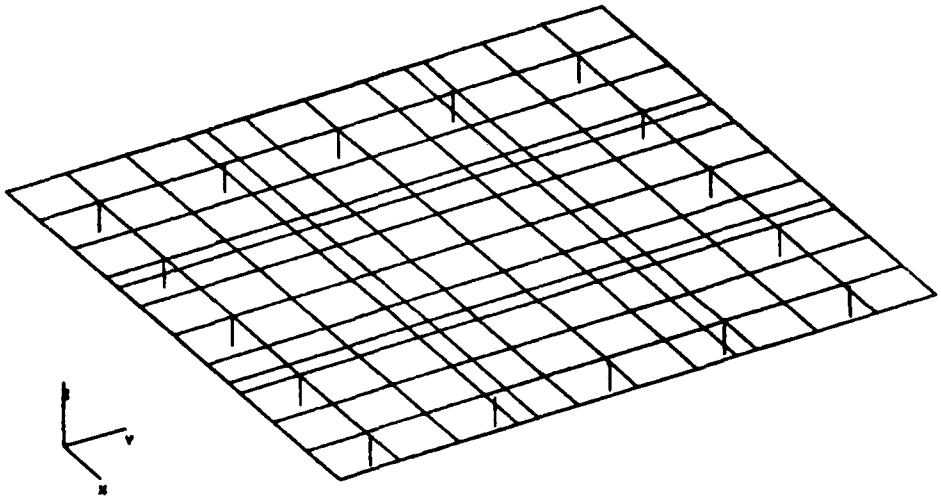
Since no electrical failures occurred, and no significant trend was noted during temperature cycling, these pull strengths were considered a normal population of pull-test data. In fact, combining these pull test results with the preliminary results gives an overall mean of 2850 g-force with a standard deviation of 872.

CONCLUSIONS

The flip-chip pull test is a viable test method to assess attachment strength. In setting a limit, a value half the mean was used as a reasonable starting point. For our samples this was 1425 g-force (using the mean of 11 tests); all the pull strengths exceeded this limit.

This was extended to other samples by considering the force on each solder bump. For the sixteen bumps on these samples the figure was 89.1 g-force/bump. The bumps were circular, 4 mils in diameter. This resulted in a bump area of 5×10^{-5} sq. in. Dividing the g-force/bump value by this area gives a value of 1781 kg-force/sq. in. as a limit that could be applied to any flip-chip.

One remaining question was the effect of sample size on the pull strength. Finite Element Modelling (FEM) was used to determine the change in the pull strength on a flip-chip with twice the length and width as the test samples (see Figure 12.5 for a description of the model). Solder bump spacing



Model Parameters

1. Dimensions of flip-chip
2. Locations and size of solder bonds
3. Chip material - silicon
4. Substrate material - alumina ceramic
5. Young's Modulus - 4.5 E6 psi
6. Poisson's Ratio - 0.25
7. Applied pressure - 1000 psi

Figure 12.5 - Flip-chip finite element model input parameters.

was kept constant (app. 16 mil) and more solder bumps were added to each side of the sample. The results showed that twice the pull strength was required when twice the number of solder bumps were included. Thus pull strength varied with solder bump area, and not with area of the chip (which increased four-fold). This motivated writing the test limit in terms of solder joint area.

The shear test results show that 5 g-force per solder bump was not a very restrictive limit for these samples. A point three standard deviations from the mean of the shear strengths measured here would be close to 1 kg-force per chip or 62.5 g-force per solder bump. A more realistic test limit might be 60 g-force per bump.

RECOMMENDATIONS

- Include the Flip-Chip Pull Test Method as part of MIL-STD-883, either as a separate method or as a condition of Method 2011.
- Change the test limit in Method 2011, Condition F from 5 g-force per solder bump to 60 g-force per solder bump.

TASK 13: HERMETICITY AND MOISTURE CONTROL EVALUATION

OBJECTIVE

To establish hermeticity criteria for large VLSI/VHSIC style packages.

METHOD

Our main concern was to determine whether present hermeticity limits and test methods would be sufficient to insure moisture control in large cavity packages. The first concern was with performing present MIL-STD-883 hermeticity tests on the sample packages. Given that a leak test method was possible, moisture intrusion in the package would be measured, correlating this rate with the measured leak rate.

The sample packages chosen for this study are listed in Table 13.1. Thirty packages representing four packages styles were used. This was an expansion of the proposed method which included only the metal hybrid packages.

A single Panametrics Mini-Mod-HT moisture sensor chip was mounted inside each package. The moisture sensing element in each chip was a porous aluminum oxide film that changed in impedance in the presence of moisture. This change was monitored with a Model 771 MM impedance bridge also manufactured by Panametrics. These devices meet the requirements of Method 1018.2, Procedure 3 of MIL-STD-883.

The die attach method for each moisture sensor is also listed in Table 13.1. The proposed plan included different die attach materials to determine the effect of enclosed organics on moisture intrusion rates, although during the actual experiment this became impossible (see Results and Conclusions sections). Electrical connections to the sensors were made with 1 mil aluminum wires.

Each Mini-Mod moisture sensor was individually calibrated following its mounting and wire-bonding (see Figure 13.1). Packages containing the sensors had wires soldered to the outer leads and were placed into a dry box. The outer lead wires were passed out of the box through a molded gasket. Dry nitrogen was passed through the box and then through a Panametrics System I Hygrometer and finally through a tube to be vented. Experiments were performed to determine the time-response and repeatability of the moisture sensors.

After calibration, the packages were baked out for 2 hours at 125°C before sealing. The parts were then sealed with a solder preform.

TABLE 13.1 - TEST SAMPLES

S/N	Style	# I/O	Internal Volume	Die Attach
1	Metal Can	58	5.24 cc	Gold-Silicon Eutectic
2	Metal Can	58	5.24 cc	Gold-Silicon Eutectic
3	Metal Can	58	5.24 cc	Non-Conductive Epoxy
4	Metal Can	58	5.24 cc	Non-Conductive Epoxy
5	Ceramic Flat Pack	132	0.26 cc	Polyimide
6	Ceramic Flat Pack	132	0.26 cc	Polyimide
7	Ceramic Flat Pack	132	0.26 cc	Non-Conductive Epoxy
8	Ceramic Flat Pack	132	0.26 cc	Non-Conductive Epoxy
9	Ceramic Flat Pack	132	0.26 cc	Gold-Silicon Eutectic
10	Ceramic Flat Pack	132	0.26 cc	Gold-Silicon Eutectic
11	Ceramic Pad Grid Array	180	0.31 cc	Polyimide
12	Ceramic Pad Grid Array	180	0.31 cc	Polyimide
13	Ceramic Pad Grid Array	180	0.31 cc	Non-Conductive Epoxy
14	Ceramic Pad Grid Array	180	0.31 cc	Non-Conductive Epoxy
15	Ceramic Pad Grid Array	180	0.31 cc	Gold-Silicon Eutectic
16	Ceramic Pad Grid Array	180	0.31 cc	Gold-Silicon Eutectic
17	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
18	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
19	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
20	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
21	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
22	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
23	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
24	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
25	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
26	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
27	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
28	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
29	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic
30	Ceramic Leadless Chip Carrier	84	0.23 cc	Gold-Silicon Eutectic

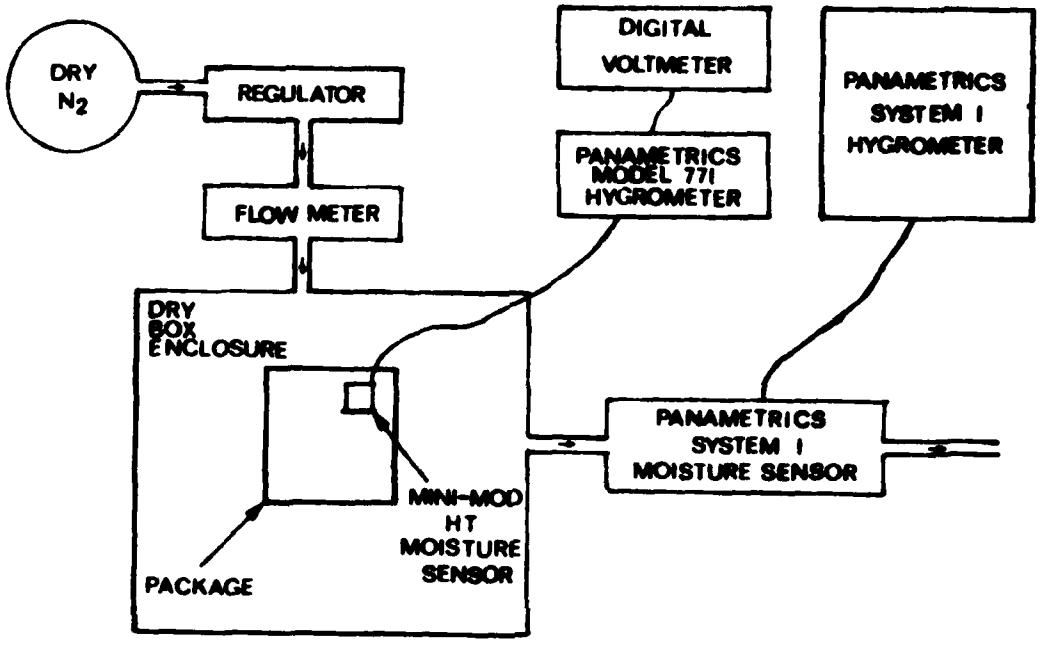


Figure 13.1 - Schematic of Apparatus Used for Moisture Sensor Calibration.

The sealed packages were placed in the dry box shown in Figure 13.1, and had moisture readings taken at dry and at room ambient moisture levels. The moisture readings from the packages were then monitored under room ambient conditions for 105 days. At this point, ten packages were selected for exposure to an environment of 95°F and 95% relative humidity (RH). Moisture sensor readings were then taken for an additional 99 days on all packages, including those at room ambient and at high humidity.

This differed from the proposed moisture resistance test which included temperature cycling during exposure to a moist environment. The moisture sensors drifted in readings (see Results section) after exposure to the thermal stress of package sealing, thus plans to do any testing that required heating the samples had to be eliminated.

Hermeticity testing of the package styles used here was accomplished successfully for similar packages in Task 3. Since no difficulty was encountered during those tests, and since the sensors showed a tendency to drift and cease function, leak testing was performed at the completion of the moisture intrusion studies. The leak rate for each package was assumed constant, which was supported by the moisture intrusion data, with the exception of the metal hybrid packages (see p. 201). Gross leak testing was performed in accordance with MIL-STD-883C, Method 1014, Test Condition C_1, Flourocarbon Gross Leak, fixed. A bomb pressure of 60 psig was applied for 2 hours. Those packages which passed gross leak testing were subsequently tested for fine leak in accordance with MIL-STD-883C, Method 1014, Test Condition A_1 He Fine Leak, fixed. A bomb pressure of 60 psig was used. The parts were subjected to a short bake-out of 10 minutes at 100°C to accelerate the allowed one-hour waiting period (see Results on p. 31). One package was then tested for gross leak in accordance with MIL-STD-883, Method 1014, Test Condition D, Dye Penetrant Gross Leak.

RESULTS

Calibration

Calibration data for Mini-Mod HT Sensors were obtained at moisture levels from 30 parts per million by volume (PPM_v) to 5000 PPM_v. Good linearity and repeatable slopes were demonstrated. Figure 13.2 shows a portion of a calibration curve for one device. Data was taken on several different days with moisture levels both slowly rising and slowly falling. No hysteresis was detected for sufficiently slow changes in moisture.

Moisture Intrusion

Following solder sealing, the sensor output voltage began to drift slowly downward for all sensors. The rate of this downward drift was seen to decay exponentially. This drift was due to the thermal cycling of the sensors

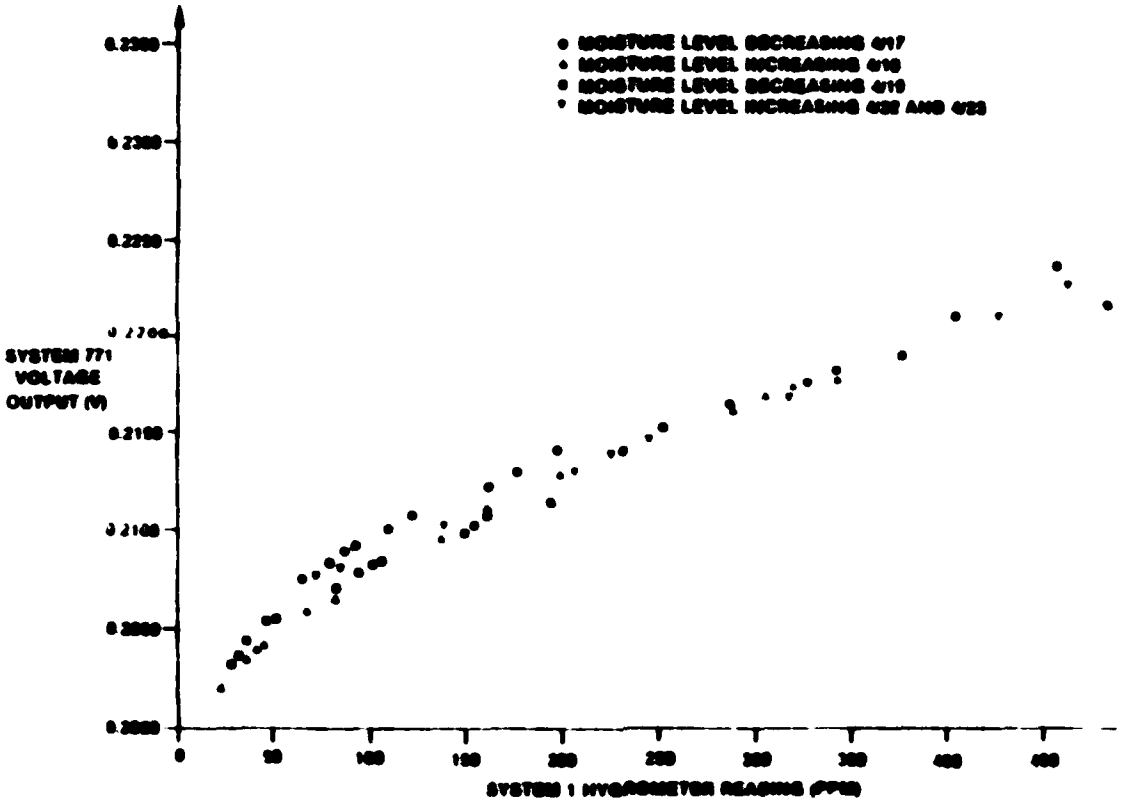


Figure 13.2 - Mini-Mod Calibration Curve for S/N 25.

during solder sealing. These readings could not have been the result of actual decreases in moisture levels because negative moisture levels were indicated. The total amount of this drift corresponded to about 200 PPM_v.

For this reason, the sealed packages were monitored at room ambient for 105 days. After this interval, most of the packages had stabilized. This stabilization permitted relative measurements to be performed although absolute moisture levels could no longer be determined due to the changes in the calibration curves. Some devices became inoperative during this study. Some of these displayed open circuit (#2, 28), and some, short circuit behavior (#15, 23).

The sealed packages were enclosed in the dry box and cycled from ambient conditions to about 50 PPM_v and back to ambient over a few days. Most of the stable moisture sensors did not respond to these changes, indicating hermetic behavior. Eight packages (#8, 9, 10, 11, 12, 13, 14, and 16) displayed dramatic changes in the detected moisture levels which tracked the dry box moisture levels exactly. This was interpreted as indicative of gross leak failures. Figure 13.3 is a graph which compares the dry box conditions to the moisture readings of two (#8, 9) of these apparent gross leaking packages. From these data it was determined that the moisture leakage rate for these packages when dry inside and exposed to ambient conditions must be greater than 2500 PPM_v/hr. These changes were much greater in magnitude than the slow downward drift. These changes were certainly indicative of a high level of moisture intrusion.

A single package (#7) was seen to exhibit a slower, but distinct, rate of moisture intrusion under room ambient conditions. Figure 13.4 shows a graph of the moisture level readings from this package as a function of time while under room ambient conditions. Room ambient levels of moisture were achieved inside this package in approximately seventy days. This package was determined to have a moisture intrusion rate of about 1.7 PPM_v/hr. When dry and exposed to room ambient conditions. None of the remaining packages exhibited any evidence of moisture intrusion during exposure to room ambient conditions for a period of 105 days.

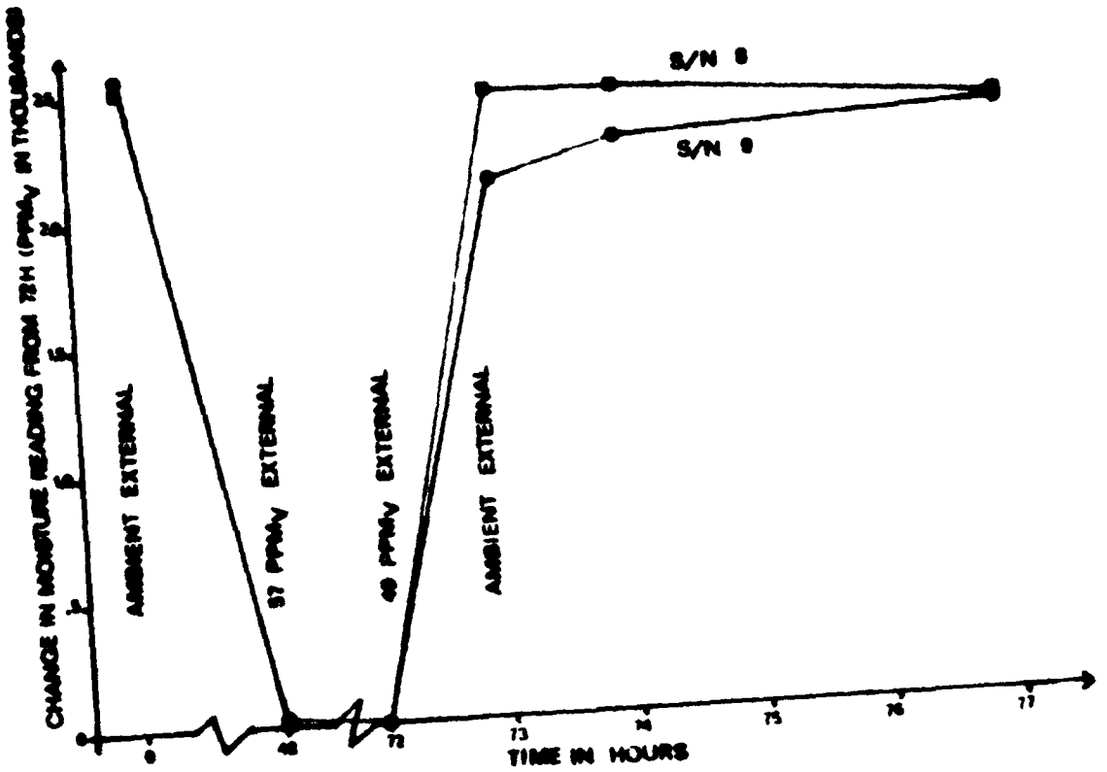


Figure 13.3 - Moisture Response of S/N 8 and S/N 9 Indicating Gross Leakage.

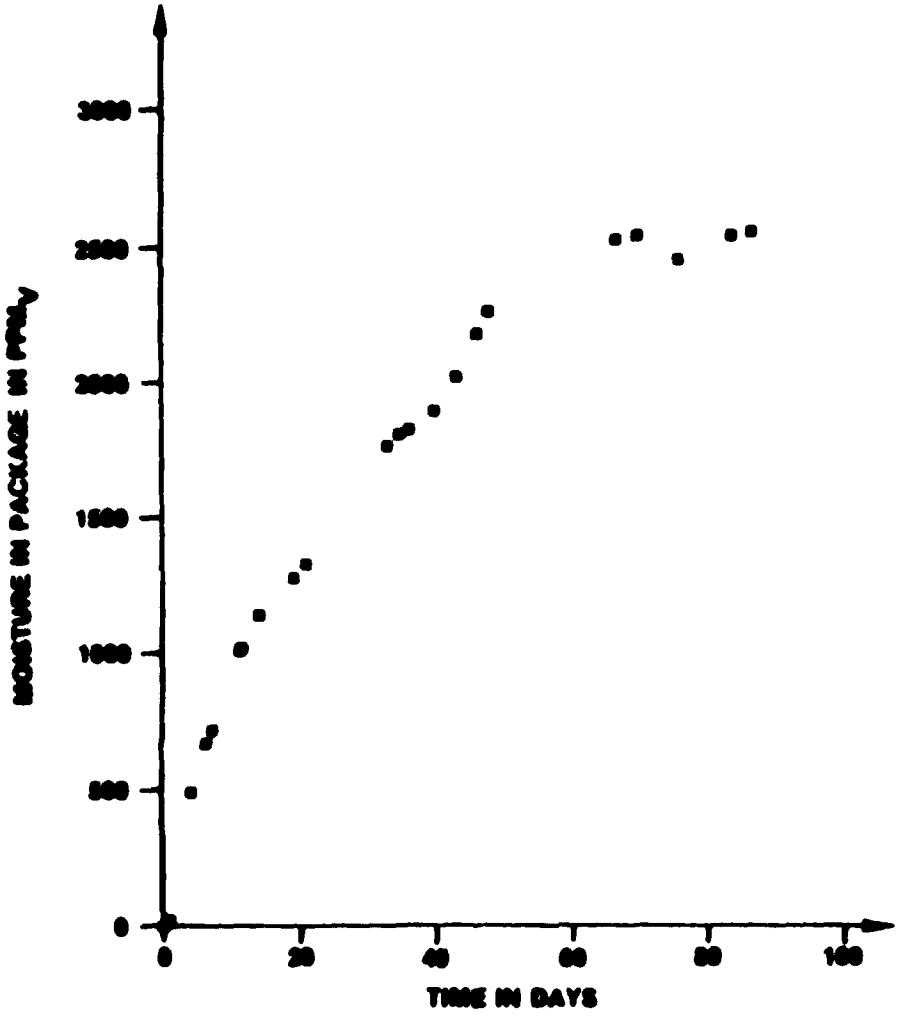


Figure 13.4 - Moisture Intrusion into S/N 7 During Exposure to Room Ambient Conditions. Moisture levels on Y-axis are for comparison. Absolute levels are probably higher.

At the end of 105 days, the original 30 packages had been divided into the following categories:

4 Dead Sensors

5 Unstable Sensors

8 Apparent Gross Leakers

1 Slow Leaker

12 Apparently Hermetic.

Of the twelve apparently hermetic packages, eight were subjected to 95% RH at 95°F ("Wet" Packages), while the other five were kept at room ambient ("Dry" Packages). Moisture readings were taken on all of these packages for another 99 days. Figure 13.5 is a graph showing the moisture reading from one of the "Dry" packages and one of the "Wet" packages as a function of time. Zero moisture change for this figure was defined as the average of all moisture readings for that package. No trend of moisture increase or decrease can be visualized in either package. No discernible increase or decrease in moisture was detected in ten of the twelve packages. Table 13.2 lists the number of data points and the standard deviation of the distribution in PPM_V for each of these ten packages. Solder sealing had altered the sensor calibrations for these devices. Therefore, the exact limits on leak rates cannot be determined.

Two of the apparently hermetic packages which were placed in the high humidity environment experienced large amounts of moisture intrusion (#1, 4). Both were large metal can type packages. This leakage was due to corrosion of the package in the region of the seal. Figure 13.6 shows photographs of these two devices after moisture intrusion was first detected. Rust is plainly visible at the seal of both packages. Degradation in hermeticity is also visible in the moisture intrusion data. Moisture levels remained low for a few weeks, then one package (#4) suddenly jumped to an exceedingly high level where it remained until the end of the test. This indicated that the formerly hermetic package had become a gross leaker. The rate of moisture intrusion into this package was greater than 54 PPM_V/Hr. Moisture intrusion data for the other package (#1) is shown in Figure 13.7. Examination of Figure 13.7 shows that the rate of moisture intrusion must have increased twice, indicated by the arrows. The final rate of moisture intrusion for this package was greater than 19 PPM_V/Hr. These rate data should be used for comparison only due to the sensor calibration shifts.

Table 13.3 summarizes all of the moisture intrusion results obtained. Those packages whose sensors became inoperative early or never stabilized are also noted.

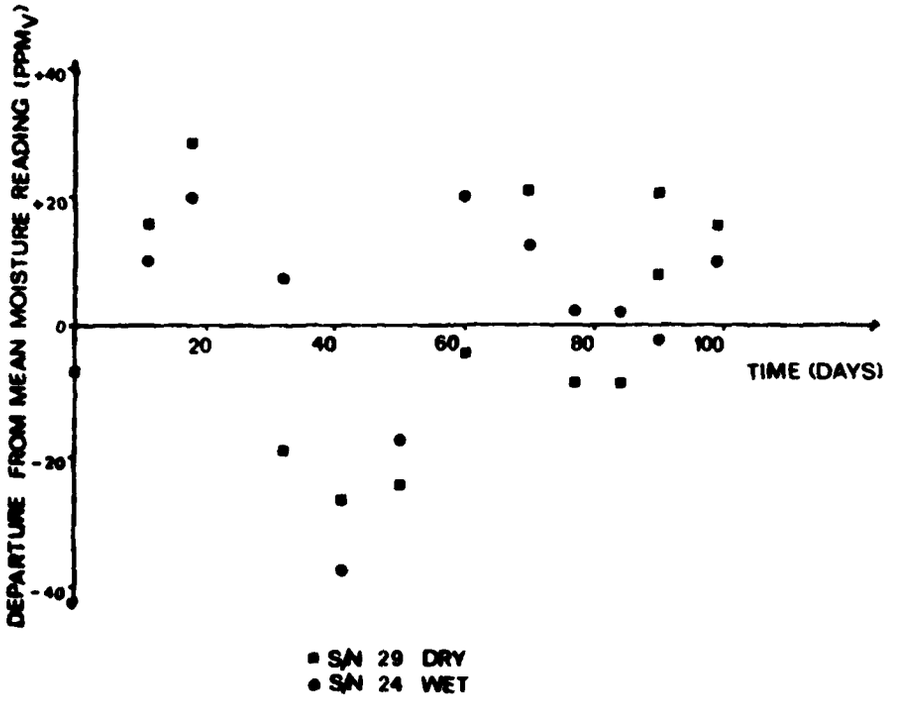


Figure 13.5 - Moisture Responses of S/N 29 Exposed to Room Ambient and S/N 24 Exposed to High Humidity.

TABLE 13.2 - MOISTURE INTRUSION DATA FOR HERMETIC PACKAGES

S/N	External Environment	Data Points	Standard Deviation in PPM_V
3	Dry	13	4
17	Wet	8	11.3
18	Wet	11	17.8
19	Wet	11	28.5
20	Wet	11	24
24	Wet	11	18.8
26	Dry	14	20.5
27	Dry	13	11.1
29	Dry	14	18
30	Wet	8	22.7

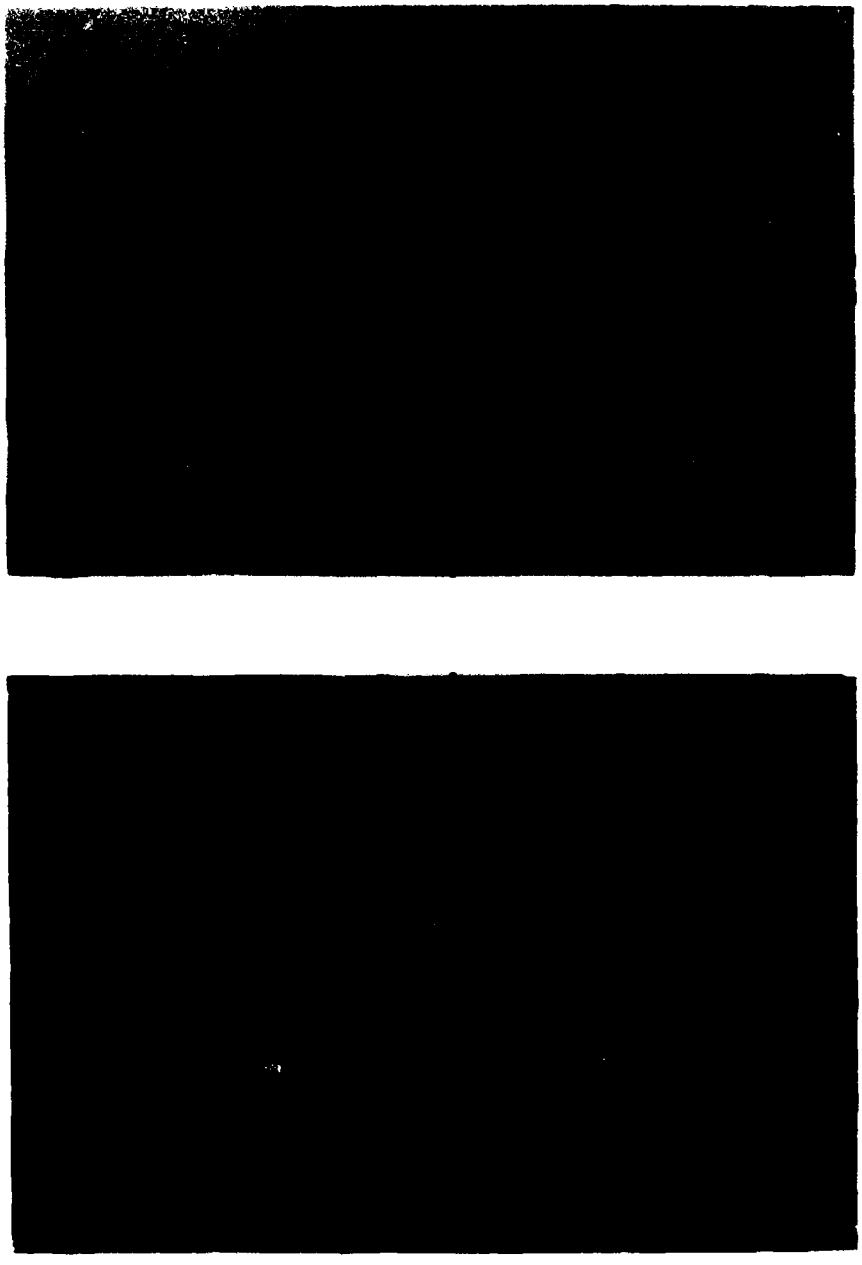


Figure 13.6 - Photographs of Packages S/N 1 and S/N 4 Showing Rust at the Seal (Actual Size).

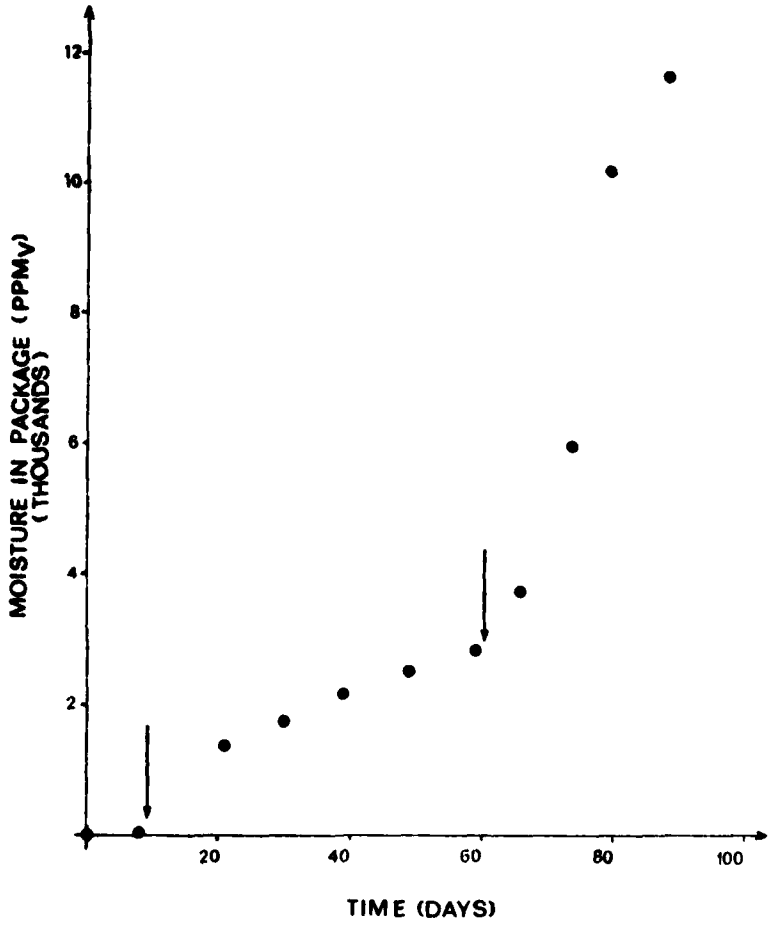


Figure 13.7 - Moisture Intrusion into S/N 1 during exposure to high humidity. Arrows indicate times at which leak rate appears to increase. Moisture levels are for comparison only. Absolute levels could not be determined due to sensor calibration shift.

TABLE 13.3 - MOISTURE INTRUSION DATA

S/N	Package Style	Environment	Moisture Intrusion Rate (PPM_V/S)
1	Metal Can	Wet	$> 5.4 \times 10^{-3}$
2	Metal Can	--	No Data - Sensor Died
3	Metal Can	Dry	$< 3 \times 10^{-6}$
4	Metal Can	Wet	1.5×10^{-2}
5	Ceramic Flat Pack	--	No Data - Unstable Sensor
6	Ceramic Flat Pack	--	No Data - Unstable Sensor
7	Ceramic Flat Pack	Dry	4.6×10^{-4}
8	Ceramic Flat Pack	Dry	$> 6 \times 10^{-1}$
9	Ceramic Flat Pack	Dry	$> 6 \times 10^{-1}$
10	Ceramic Flat Pack	Dry	$> 6 \times 10^{-1}$
11	Ceramic Pad Grid Array	Dry	$> 6 \times 10^{-1}$
12	Ceramic Pad Grid Array	Dry	$> 6 \times 10^{-1}$
13	Ceramic Pad Grid Array	Dry	$> 6 \times 10^{-1}$
14	Ceramic Pad Grid Array	Dry	$> 6 \times 10^{-1}$
15	Ceramic Pad Grid Array	--	No Data - Sensor Died
16	Ceramic Pad Grid Array	Dry	$> 6 \times 10^{-1}$
17	Ceramic Leadless CC	Wet	$< 3 \times 10^{-6}$
18	Ceramic Leadless CC	Wet	$< 3 \times 10^{-6}$
19	Ceramic Leadless CC	Wet	$< 3 \times 10^{-6}$
20	Ceramic Leadless CC	Wet	$< 3 \times 10^{-6}$
21	Ceramic Leadless CC	--	No Data - Unstable Sensor
22	Ceramic Leadless CC	--	No Data - Unstable Sensor
23	Ceramic Leadless CC	--	No Data - Sensor Died
24	Ceramic Leadless CC	Wet	$< 3 \times 10^{-6}$
25	Ceramic Leadless CC	--	No Data - Unstable Sensor
26	Ceramic Leadless CC	Dry	$< 3 \times 10^{-6}$
27	Ceramic Leadless CC	Dry	$< 3 \times 10^{-6}$
28	Ceramic Leadless CC	--	No Data - Sensor Died
29	Ceramic Leadless CC	Dry	$< 3 \times 10^{-6}$
30	Ceramic Leadless CC	Wet	$< 3 \times 10^{-6}$

Leak Test Results

Gross leak testing was performed on all packages (except #2 which died early) per MIL-STD-883C, Method 1014, Test Condition C_1, Fluorocarbon Gross Leak, fixed. Parts were bombed at 60 psig for 2 hours.

Eighteen packages which passed gross leak test were tested per MIL-STD-883C, Method 1014, Test Conditon A_1, Helium Fine Leak, fixed. A bomb pressure of 60 psig was used and the part was baked for 10 minutes at 100°C to accelerate the 1-hour allowed waiting period. Leak rates were measured and recorded for all packages.

One package (#10) was an apparent gross leaker from moisture intrusion data and yet it was reported to pass fine and gross leak testing. A helium leak rate of 1.8×10^{-8} atm-cc/s was reported. Visual examination without magnification of this part showed large voids in the seal. Gross leak testing per MIL-STD-883C, Method 1014, Test Condition D, Dye Penetrant Gross leak, was then performed. Large amounts of dye were inside the cavity. This package was then diagnosed as a gross leaker.

To perform an analysis, all moisture intrusion data was converted to units of g/s intrusion of water. This absolute measure of moisture intrusion should relate directly to absolute helium leak rate expressed in atm-cc/s. All of the packages in this study were sealed with solder preforms, thus the effects of package geometry should not be significant. Though seal areas and package volumes may vary, any existing leakage path would exist for both helium and water. Thus, it is reasonable to expect a correlation between absolute helium leak rates and absolute moisture intrusion rates.

Table 13.4 summarizes all of the helium leak rate data and the moisture intrusion data converted into absolute units. Figure 13.8 is a plot of $\log_{10}$ of the absolute moisture intrusion rate versus $\log_{10}$ of the measured helium leak rate. All gross leakers were assigned a helium leak rate of $> 10^{-5}$ atm-cc/s because this is the upper limit of measurement on our equipment. Two vertical lines are drawn on Figure 13.8. The right hand line corresponds to a helium leak rate of 5×10^{-8} atm-cc/s. This is the acceptable limit per MIL-STD-883. The left hand line corresponds to a helium leak rate of 10^{-8} atm-cc/s. The data point corresponding to package #7 falls between these lines. This package is,therefore,considered to be hermetic by MIL-STD-883. However, moisture intrusion data shows that this package achieved ambient levels of moisture in just 70 days at room ambient, which is cause for some concern.

Another concern is raised by the experience of the rusting packages. These packages would likely have passed fine leak testing prior to humidity exposure, yet they became gross leakers after only a few months.

TABLE 13.4 - MOISTURE INTRUSION AND HELIUM LEAK DATA IN ABSOLUTE UNITS

S/N	Moisture Intrusion Rate (g/s)	Helium Leak Rate (atm-cc/s)
1	> 2.3×10^{-11}	> 10^{-5}
2	No Data	No Data
3	< 1.3×10^{-14}	6.2×10^{-9}
4	> 6.3×10^{-11}	> 10^{-5}
5	No Data	2.7×10^{-9}
6	No Data	1.5×10^{-9}
7	9.6×10^{-14}	3.5×10^{-8}
8	> 1.3×10^{-10}	> 10^{-5}
9	> 1.3×10^{-10}	> 10^{-5}
10	> 1.3×10^{-10}	> 10^{-5}
11	> 1.5×10^{-10}	> 10^{-5}
12	> 1.5×10^{-10}	> 10^{-5}
13	> 1.5×10^{-10}	> 10^{-5}
14	> 1.5×10^{-10}	> 10^{-5}
15	No Data	> 10^{-5}
16	> 1.5×10^{-10}	> 10^{-5}
17	< 5.6×10^{-16}	1.6×10^{-9}
18	< 5.6×10^{-16}	4.6×10^{-9}
19	< 5.6×10^{-16}	0.4×10^{-9}
20	< 5.6×10^{-16}	1.8×10^{-8}
21	No Data	1.9×10^{-9}
22	No Data	6.5×10^{-9}
23	No Data	> 10^{-5}
24	< 5.6×10^{-16}	0.8×10^{-9}
25	No Data	1.3×10^{-9}
26	< 5.6×10^{-16}	1.5×10^{-9}
27	< 5.6×10^{-16}	0.7×10^{-9}
28	No Data	0.7×10^{-9}
29	< 5.6×10^{-16}	0.7×10^{-9}
30	< 5.6×10^{-16}	1.1×10^{-9}

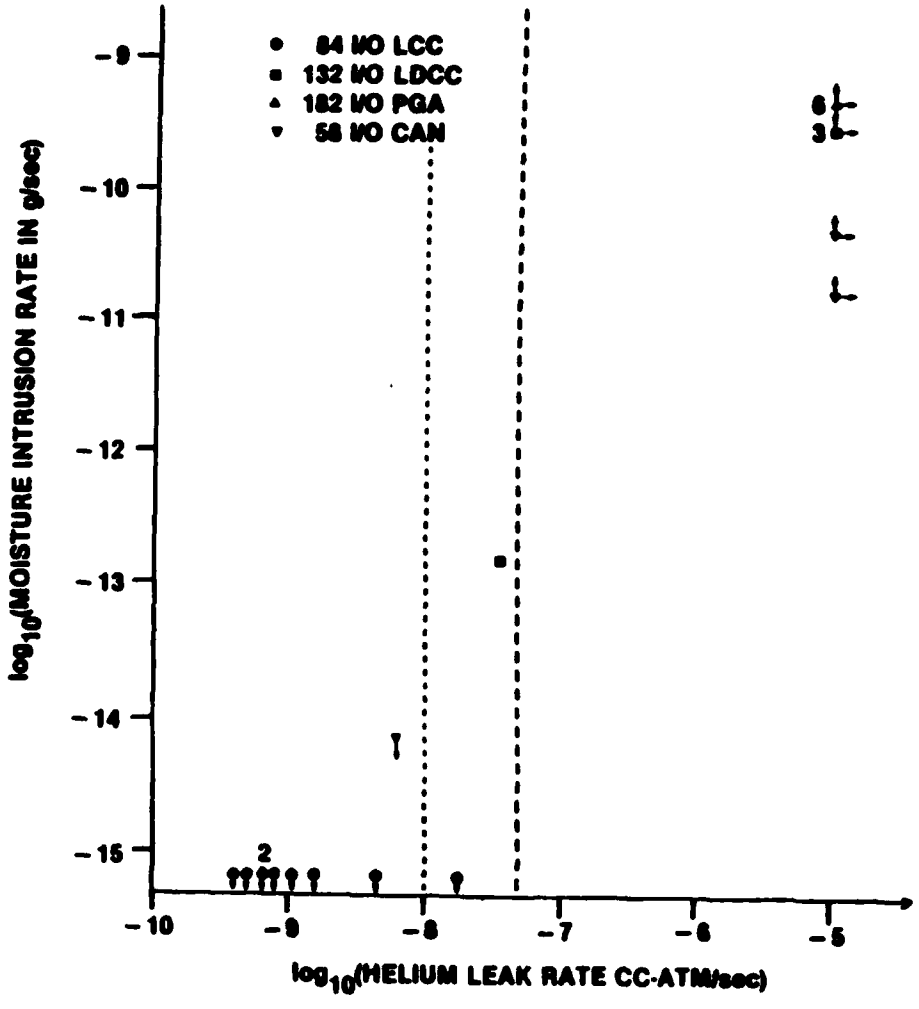


Figure 13.8 - A log-log plot of absolute moisture intrusion rates versus measured helium leak rates. Small numerals beside data points indicate a number of superimposed data points. Small arrows indicate that the data is bounded in that direction for that data.

CONCLUSIONS

The following conclusions can be made from the results of the experiment:

- A correlation exists between helium leak rates as determined by MIL-STD-883C, Method 1014, Test Condition A_1, and moisture intrusion rates.
- One package with a measured helium leak rate between 5×10^{-8} and 1×10^{-8} atm-cc/s reached room ambient levels of moisture in a few months.
- Packages with a measured helium leak rate less than 10^{-8} atm-cc/s will take at least a year to have their internal moisture level increase by 100 PPM_V.
- Corrosion of package seals can compromise hermeticity. Although this was a side issue in this study, it was clear that proper corrosion protection must be provided for all package seals appropriate to this environment.
- Panametrics Mini-Mod sensors should not be subjected to temperature excursions if at all possible. Any such sensors should be recalibrated following any temperature excursions.

RECOMMENDATION

- Consider tightening the acceptance limit for MIL-STD-883, Method 1014, Test Condition A_1 from 5×10^{-8} to 1×10^{-8} atm-cc/s. Although it is difficult to draw strong conclusions from a single data point, the indication is that moisture can penetrate an "acceptable" package within a relatively short amount of time. Additional study in this area is recommended.

APPENDIX

MIL-STD-883 FORMAT

TEST METHODS

METHOD 2003.X

SOLDERABILITY

Change:

1. Paragraph 3.4

   From: "...the dwell time in the solder bath shall be 5 ± 1/2 seconds, unless other wise specified."

   To: "...the dwell time in the solder bath shall be 5 ± 1/2 seconds, unless otherwise specified. In the case of high mass, leadless packages only, a dwell time of 10 ± 1/2 seconds may be specified."

2. Paragraph 4

   From: " d. Solder dip (see 3.4.)."

   To: " d. Solder dip and dwell time (see 3.4)."

METHOD 20XX.1

PIN-GRID PACKAGE DESTRUCTIVE LEAD PULL TEST

1. PURPOSE. This method provides a test for determining the integrity of pin-grid type package leads by measuring the capability of the package leads to withstand an axial force.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for supplying the specified stress to the package lead. A calibrated measurement and indication of the applied stress in grams-force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of $\pm$5 percent or $\pm$0.25 gf, whichever is greater.

3. PROCEDURE. Unless otherwise specified, the stress shall be applied to three leads or 10 percent of the leads (whichever is greater) randomly selected from each device prior to start of test. Tension only shall be applied, without shock, to each lead to be tested in a direction parallel to the axis of the lead. The tension shall be applied at a rate of 500 gf/s $\pm$ 100 gf/s, and shall continue to destruction. The tension shall be applied as close to the end of the lead as possible.

3.1 Failure criteria. The minimum acceptable lead pull strength shall be 1.70×10^7 grams-force per square inch of cross-sectional Kovar lead area (e.g., the minimum pull strength of a lead with a cross-sectional area of 2.0×10^{-4} in^2 will be 3400 grams-force). Other lead metals will need appropriate test limits.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Number and selection of leads, if different from above.
b. Measured lead pull strength and minimum required pull strength, if different from above.

METHOD 20XX.1

CERAMIC CHIP CARRIER BOND STRENGTH (DESTRUCTIVE PUSH TEST)

1. PURPOSE. The purpose of this test method is to measure strengths of bonds external to leadless microelectronic packages (e.g., solder bonds from chip carrier terminals to substrate or wiring board).

2. APPARATUS. The apparatus for this test method shall consist of suitable equipment for applying the specified stress to the device terminals. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is greater.

3. PROCEDURE. The test shall be conducted using the test procedure which follows. All push tests shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. A minimum of 4 chip carriers (or use all chip carriers if 4 are not available) on each of a minimum of 2 completed substrates or wiring boards shall be used. Where there is any adhesive, encapsulant or other material under, on or surrounding the chip carrier such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

3.1 Test samples. The following conditions for selection of test samples shall apply:

a. The sample of packages for this test shall be taken at random from the same chip carrier population as that used in the completed devices that they are intended to represent.
b. The packages for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.
c. The test package substrates shall be processed and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1.1 Sample preparation. Substrates must be prepared as follows:

a. A roughly circular area comprising 50%, +5%/-0% of the bonded side of each package to be tested must be exposed by either end-mill drilling of the test substrate or other suitable means. If it is not possible to expose the ceramic in this manner, the packages shall be bonded onto test substrates into which the proper hole(s) and hole size(s) has (have) been manufactured, providing all other conditions of 3.1 have been met.

b. Suitable support must be provided for the test substrate so that there is a minimum of flexure of the substrate during the test. This support, if necessary, may be provided by bonding the substrate to a rigid metal plate having a hole pattern matching that of the test substrate.

c. A cylindrical rigid metal test post must be prepared for each hole size, which will be inserted through the support plate and test substrate holes. The post will be used to transmit the specified stress from the stress-source equipment to the exposed package surface. The diameter of the post shall be 85% (+5%/-0%) of the corresponding test hole diameter. The length of the post shall be sufficient to extend 1 in. (+100%/-0%) from the open end of the test hole when the post is inserted completely into the hole.

3.2 Testing. The test shall be performed in the following manner:

a. A single package shall be pushed during each test sequence.
b. A layer of teflon tape per MIL-T-27730 or equivalent shall be placed between the exposed chip carrier surface and the test post prior to testing.
c. Insert test post into test hole. The contact of the test post to the ceramic chip carrier shall be made without appreciable impact (≤.1 in/min). With the stressing element of the test equipment traveling at a constant rate of 0.02 + 1% in/sec., apply sufficient force to chip carrier (through test post) to break all chip carrier to substrate bonds on at least three edges of chip carrier under test. When failure occurs, the force at the time of failure and the failure category shall be recorded. Any test resulting in the fracturing of either the chip carrier or test substrate shall be considered unacceptable. The data from the test shall be discarded, and the test performed again.

3.3 Failure criteria. Any push test which results in separation with a bond strength of less than 30 kg-force per linear inch (1180 g-force per lin. mm) of solder pad width shall constitute a failure. The bond strength shall be determined by dividing the separating force by the total of the solder pad widths as measured on the substrate at the package edge, in a direction parallel to the package edge.

3.3.1 Failure category. Failure categories are as follows. When specified, the stress required to achieve separation and the predominant category of separation shall be recorded:

a. Device fracture.
b. Failure in package-bond interface.
c. Terminal break at point not affected by bonding process.

d. Failure in bond-substrate conductor interface.
e. Conductor lifted from board or substrate.
f. Fracture within board or substrate.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Minimum bond strength if other than specified in 3.3 or details of required strength distributions if applicable.
b. LTPD or selection and number of devices to be tested on each substrate, if other than 4.
c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.3.1).

METHOD 20XX.1

ULTRASONIC INSPECTION OF DIE ATTACH

1. PURPOSE. The purpose of this examination is to non-destructively detect unbonded regions and voids in the die attach material of semiconductor devices through the measure of acoustic continuity. It establishes methods and criteria for ultrasonic inspection of semiconductor devices.

NOTE: For certain die attach materials, a dramatic distinction between well-bonded and poorly bonded conditions may be difficult to achieve. This factor should be considered in relation to the design of each device when application of this test method is specified.

2. APPARATUS. The apparatus and materials for this test shall include:

a. Ultrasonic imaging equipment with a test frequency sufficient to penetrate to the die attach interface. The test frequency and focal distance shall be adequate to detect voids as small as 0.0254 mm (0.001 inch) in diameter.
b. Output device - A hard copy recording unit (C-Scan) or other directly recording device (computer storage) shall be used to produce an image for analysis (manual or automated). The dynamic range of the output image shall be at least sixteen discernable colors or levels of grey. The image shall be large enough to be viewed at 10X or lower magnification.
c. Ultrasonic Detector - shall be capable of detecting an acoustic signal which enters the back or bottom of the package and is reflected by the die attach interface. This mode of imaging shall be used where the opening of a sealed, hermetic device is undesirable.

3. PROCEDURE. The pulse/receiver/gate/peak detector and live scan recorder settings (when used) shall be selected or adjusted as necessary to obtain satisfactory images and achieve maximum image details within the sensitivity requirements for the device or defect features the test is directed toward.

3.1 Mounting and views. The devices shall be mounted in the holding tank so that the devices are not damaged or contaminated and are in the proper plane as specified. The devices may be mounted in any type of fixture provided the fixtures do not block the view from ultrasonic transducer to any portion of the body of the device. The coupling fluid in the holding tank shall be distilled water or other suitable non-corrosive liquid.

3.1.1 Views. All devices, unless otherwise specified, shall have one view made with the acoustic signal penetrating the device in a direction perpendicular to the plane of the die attach, and for which there is acoustic continuity from the case exterior surface to the die attach interface (generally, the Y1 direction with the die attach parallel to the XZ plane). For devices with no sealed air gap above the active surface of the semiconductor element (unlidded devices), a view made with the acoustic signal directed from the active surface of the semiconductor element to the die attach interface may be specified.

3.2 Recording and marking. The acoustic image, unless otherwise specified, shall be printed by equipment using dry electrosensitive paper and with a resolution of 150 data elements per inch nominal. The image shall be identified by unambiguously marking the paper on which the image is printed with the following information:

a. Device manufacturer's name or code identification number.
b. Device type or part number.
c. Production lot number or date code or inspection lot number.
d. Ultrasonic image view number and date.
e. Device serial or cross reference numbers, where applicable.
f. Ultrasonic laboratory identification, if other than device manufacturer.

3.2.1 Non-print techniques, when specified. The use of other than paper recording techniques is permitted if permanent records are not required and the equipment is capable of producing results of equal quality when compared to printed recording techniques, and all requirements of this method are complied with, except those pertaining to the actual recording.

3.2.2 Serialized devices. When device serialization is required, each device shall be readily identified by a serial number. They shall be imaged in consecutive, increasing serial order. When a device is missing, the blank space shall contain the serial number or other marking to readily identify and correlate ultrasonic image data. When large skips occur within serialized devices, the serial number of the last device before the skip and the first device after the skip may be used in place of large physical spacing of the devices.

3.2.3 Special device marking. When specified (see 4B), the devices that have been imaged and found acceptable shall be identified with a blue dot on the external case. The blue dot shall be approximately 1/16 inch in diameter. The color selected from FED-STD-515 shall be any shade between 15102-15123 or 25102-25109. The dot shall be placed so that it is readily visible but shall not obliterate other device markings.

3.3 Tests. Acoustic frequency gate settings, receiver attenuation, and other equipment settings shall be selected to achieve resolution of 0.0254 mm (0.001) in major dimension, image only the signal reflected from the die attach interface, and to demark image features with as great contrast as possible. Ultrasonic images shall be made for each view required (see 4).

3.4 Operating personnel. Personnel who will perform ultrasonic inspection shall have training in ultrasonic imaging procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. The following minimum vision requirements shall apply for visual acuity of personnel inspecting images:

a. Distant vision shall equal at least 20/30 in both eyes, corrected or uncorrected.
b. Near vision shall be such that the operator can read Jaeger type No. 2 at a distance of 16 inches, corrected or uncorrected.
c. Vision tests shall be performed by an oculist, optometrist, or other professionally recognized personnel at least once a year. Personnel authorized to conduct ultrasonic imaging tests shall be required to pass the vision tests specified in 3.4a and b.

3.5 Interpretation of ultrasonic images. Ultrasonic images shall be inspected to determine that each device conforms to this standard and defective devices shall be rejected. Interpretation of the image shall be made under moderate light level conditions without a glare on the recording paper's surface. The image shall be viewed at a magnification between 1X and 10X.

3.6 Reports of records.

3.6.1 Reports of inspection. For class S devices, or when specified for other device classes, the manufacturer shall furnish inspection reports with each shipment of devices. The report shall describe the results of the ultrasonic inspection, and list the purchase order number or equivalent identification, the part number, the date code, the quantity inspected, the quantity rejected, and the date of test. For each rejected device, the part number, the serial number, when applicable, and the cause for rejection shall be listed.

3.6.2 Image and report retention. When specified, the manufacturer shall retain a set of the ultrasonic images and a copy of the inspection report. These shall be retained for the period specified.

3.7 Examination and acceptance criteria. In the examination of devices, the following aspects shall be considered unacceptable die mounting, and devices that exhibit any of the following defects shall be rejected:

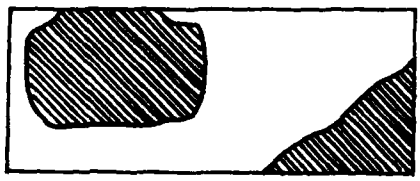
Voids - when imaging devices ultrasonically, certain types of mounting material may not give true representation of voids. When such devices are inspected, the mounting shall be noted on the inspection report.

1. Contact area voids in excess of 50% of the total intended contact area.
2. A single void which exceeds 15% of the intended contact area, or a single corner void in excess of 10% of the total intended contact area (see Figure 20XX-1).
3. When the image is divided into four equal quadrants by bisecting both pairs of opposite edges, any quadrant exhibiting contact area voids in excess of 70% of the intended quadrant contact area (see Figure 20XX-1).

In case of dispute, the percent of voiding shall be determined by actual measurement from the image.

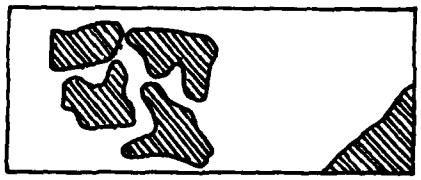
4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Number of views, if other than indicated in 3.1.1.
b. Marking, if other than indicated in 3.2 and marking of samples to indicate they have been ultrasonically imaged, if required (3.2.3).
c. Defects to be sought in the samples and criteria for acceptance or rejection, if other than indicated in 3.7.
d. Image and report retention, if applicable (see 3.6.2).
e. Test reports when required for class B or S devices.



Reject: Single void larger than 15% of total intended contact area.

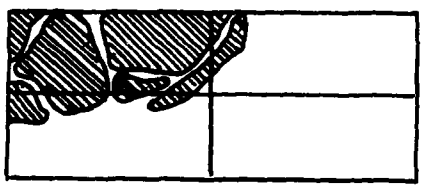
Reject: Corner void larger than 10% of total intended contact area.



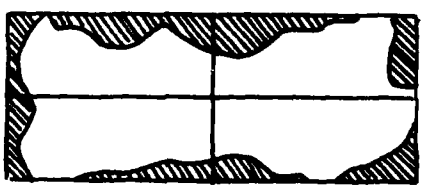
Accept: No single void larger than 15% of total intended contact area.

Accept: Corner void of area less than 10% total intended contact area.

 = VOID or Unbonded Area.



Reject: Quadrant more than 70% unbonded.



Accept: All quadrants less than 70% unbonded.

Figure 20XX.1 - Ultrasonic Image Accept/Reject Criteria.

METHOD 30XX.1

MICROELECTRONICS PACKAGE DIGITAL SIGNAL TRANSMISSION

1. PURPOSE. This method establishes the means of evaluating the characteristic impedance, capacitance, and delay time of signal lines in packages used for high frequency digital integrated circuits. It is intended to assure a match between circuit performance and interconnecting wiring to minimize signal degradation.

1.1 Definitions.

1.1.1 Characteristic impedance. The impedance that a section of transmission line exhibits due to its ratio of resistance and inductance to capacitance.

1.1.2 Delay time. The time delay experienced when a pulse generated by a driver with a particular drive impedance is propagated through a section of transmission line.

1.2 Symbols.

R: Resistance
L: Inductance
C: Capacitance
t_{pd}: Propagation delay time

2. APPARATUS. The apparatus for transmission performance measurements shall include a suitable Time Domain Reflectometer (TDR) (See Sec. 2.1) and DC resistance measuring equipment (See Sec. 2.2).

2.1 Time domain reflectometer. The TDR used for this test shall have a system rise time for the displayed reflection that is not less than 5 times and preferably 10 times the rise time (Method 3004.1) for the candidate integrated circuits to be packaged. Interconnecting cables and fixtures shall be designed such that this ratio is not degraded due to reflections and ringing in the test setup.

2.2 DC resistance. DC resistance measuring equipment and probe fixtures are required to be capable of measuring the resistance of the package leads and the chip-to-package interconnect media with an accuracy of $\pm$ 10% of the actual value including errors due to the mechanical probing interface contact resistance.

3. PROCEDURE. The test equipment configuration shall be as shown in Figure 30XX.1-1 using a time domain reflectometer as specified (See 2). The characteristic impedance (Z_o), propagation time (t_{pd}), resistance and load capacitance (C_L) shall be measured for all representative configurations as determined by a review of the package drawings and the intended applications (See 3.2 through 3.3).

3.1 General considerations.

3.1.1 TDR measurements. Accurate measurement of transmission performance of a package pin using a TDR requires careful design and implementation of adapter fixtures to avoid reflections due to transmission line discontinuities in the cables and junctions between the TDR and the package being tested. The accuracy of the measurement will be enhanced if the coaxial cable used to interface to the package is of a characteristic impedance as close as possible to the package pin impedance. The interface to the package should be a soldered connection and mechanical design of the actual coax-to-package interface must minimize the length of the uncontrolled impedance section. Stripline interfaces are the best method for surface-mount package styles.

3.1.2 Test configurations. Obtaining a good high frequency ground is important. Connection of the package ground plane (if the package design has one) to the test set-up ground plane should be accomplished with a pin configuration similar to actual usage in the intended package applications.

Pin selection for testing may vary according to package complexity. For packages with very symmetrical pin configurations only a few pins need be tested but configurations must include pins adjacent and non-adjacent to the ground pins. Packages with complex wiring and interconnect media should be tested 100%.

3.2 Test procedure for package transmission characteristics. Using a section of coaxial cable of known, calibrated characteristic impedance (Z_{Ref}) as a reference measure, the minimum (Z_{Min}), maximum (Z_{Max}), and average (Z_o) values of reflection coefficient (ρ) for the section of line on the TDR display that has been carefully determined to be the package pin (Locate using zero-length short circuits).

Calculate characteristic impedance (Z_o) for each of the cases from the formula:

$$Z_o = Z_{Ref} \times \frac{(1+\rho)}{(1-\rho)}$$

3.2.2 Delay time measurement. From the TDR display of 3.2.1, measure the time difference in picoseconds from the point identified as the start of the exterior package pin (t_1) to the chip interface point (t_2) ($\Delta t = t_1 - t_2$)

From the package design drawings, determine the physical length of the package run (L)

$$\text{Time delay } t_{pd} = \frac{\Delta t}{L}$$

3.2.3 Load capacitance calculation.

$$\text{Load capacitance } C_L = \frac{t_{pd}}{Z_o}$$

3.2.4 Load inductance calculation.

$$\text{Load inductance (series)} = \frac{(t_{pd})^2}{C_L}$$

3.3 Series resistance measurement.

Using the test configurations of Figure 30XX.1-2, separately measure the DC resistance of the chip-to-package interface media (R_M) and the package lead (R_L).

4. SUMMARY. The following details, when applicable, shall be specified in the applicable procurement document:

a. Z_{Max}
b. Z_{Min}
c. Z_o (max)
d. Z_o (min)
e. t_{pd} (max)
f. t_{pd} (min)
g. C_L (max)
h. C_L (min)
i. L_L (max)
j. L_L (min)
k. R_M (max)
l. R_M (min)
m. R_L (max)
n. R_L (min)
o. Package pins to be tested
p. Package ground configuration

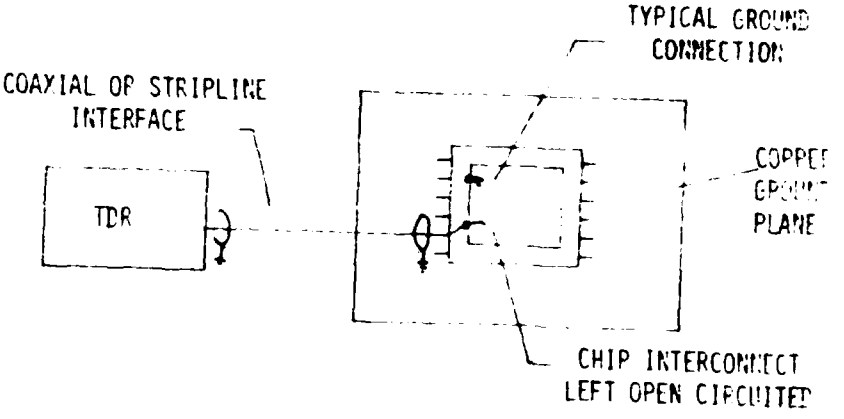
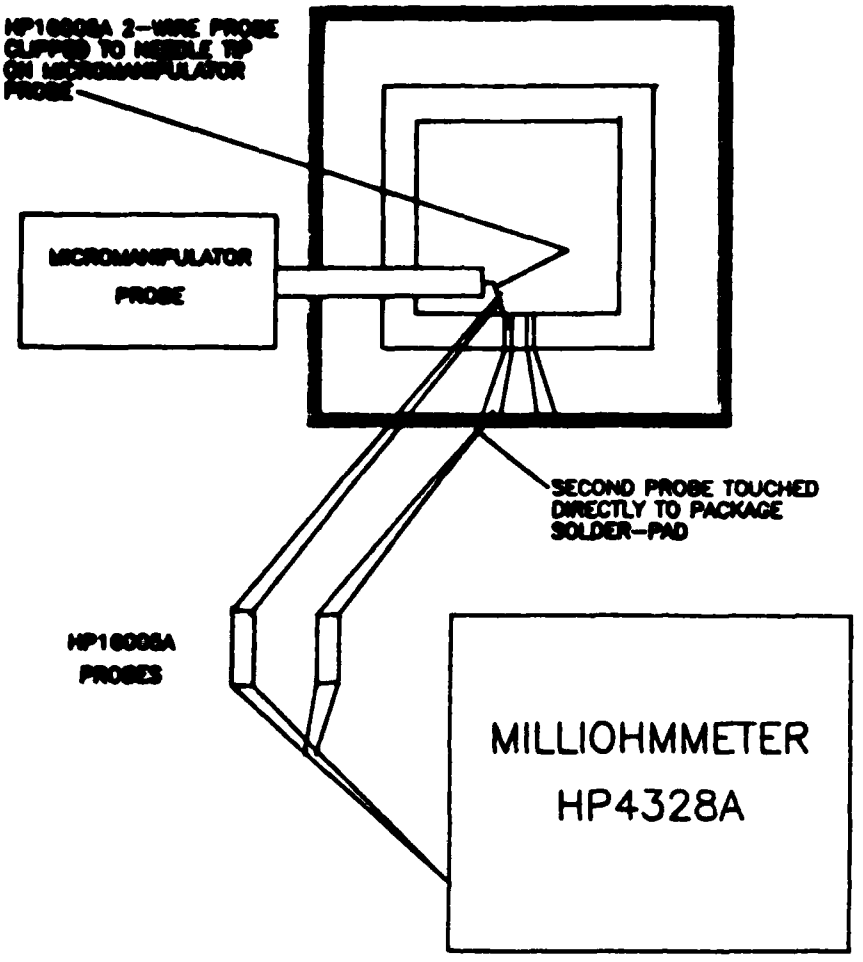


Figure 30XX.1-1 - Time Domain Reflectometer Test Setup.



TEST SETUP FOR DC RESISTANCE
USING A MILLIOHMMETER

Figure 30XX.1-2 - Test Setup for DC Resistance Using a Milliohmmeter.

METHOD 30XX.1

CROSSTALK MEASUREMENTS FOR DIGITAL MICROELECTRONICS DEVICE PACKAGES

1. PURPOSE. This method establishes the means of measuring the level of cross-coupling of wideband digital signals and noise between pins in a digital microcircuit package. The method may be used to gather data that are useful in the prediction of the package's contribution to the noise margin of a digital device. The technique is compatible with multiple logic families provided that the drive and load impedance are known.

1.1 Definitions.

1.1.1 Crosstalk. Signal and noise waveforms coupled between isolated transmission lines, in this case, package conductors.

1.1.2 Coupling capacitance. The effective capacitance coupling between a pair of conductors in a package as measured by the time constant of the charge pulse applied on one line and measured on the other.

1.1.3 Noise pulse voltage. The voltage of a crosstalk measured at the minimum noise pulse width as measured on a receiver input line.

1.1.4 Peak noise voltage. The peak value of the noise pulse measured on a receiver input line.

1.2 Symbols. The following symbols shall apply for the purpose of this test method and shall be used in accordance with the definitions provided (See 1.2.1 and 1.2.2).

1.2.1 Logic levels.

V_{OL}(max): The maximum output LOW level specified in a logic system.

V_{OH}(min): The minimum output HIGH level specified in a logic system.

V_{IL}(max): The maximum allowed inpuc LOW voltage level in a logic system.

V_{IH}(min): The minimum allowed input HIGH level in a logic system.

1.2.2 Noise pulse width.

t_{PL}: The LOW level noise pulse width, measured at the V_{IL} (max) level. (Ref. Method 3013.1)

t_{PH}: The HIGH level noise pulse width measured at the V_{IH} (min) level. (Ref. Method 3012.1)

1.2.3 Transition times. (Ref. Method 3004.1)

t_{tLH}: rise time. The transition time of the output from the 10 percent to the 90 percent of the HIGH voltage levels with the output changing from LOW to HIGH.

t_{tHL}: fall time. The transition times from 90 percent to 10 percent of the HIGH voltage level with the output changing from HIGH to LOW.

1.2.4 Crosstalk parameters.

C_C: coupling capacitance (see 1.1.2).

V_N: noise pulse voltage (see 1.1.3).

V_{NPK}: peak noise voltage (see 1.1.4).

2. APPARATUS. The apparatus used for crosstalk measurements shall include a suitable source generator (see 2.1), wideband oscilloscope (see 2.2), low capacitance probe (see 2.3) and load resistors (see 2.4).

2.1 Source generator. The source generator for this test shall be capable of duplicating (within 5%) the transition times, V_{OH} and V_{OL} levels of the logic system(s) being considered for application using the package style under evaluation. The source generator shall have a nominal characteristic source impedance of 50 ohms.

2.2 Wideband oscilloscope. The oscilloscope used to measure the crosstalk pulse shall have a display rise time that is less than 20% of the rise time of the logic systems being considered for application in the package style under evaluation. A sampling-type oscilloscope is recommended.

2.3 Low capacitance probe. The interface between the oscilloscope and the unit under test shall be a high impedance low capacitance probe. The probe impedance shall be 10[illegible] ohms, minimum,and the capacitance shall be 5 picofarads, maximum,unless otherwise specified in the procurement document.

2.4 Load resistors. The load resistors specified for this test shall be low inductance, low capacitance, chip style resistors with a tolerance of ±5%. Load resistor value(s) shall be specified by the procurement document to match the load impedance levels of the application logic family for a single receiver load.

3. PROCEDURE. The test equipment configuration shall be as shown in figure 30XX.1-1 using a source generator, oscilloscope, probe and loads as specified (see 2). Measurements shall be made of coupling capacitance, (see 3.2) and if required by the procurement document, of noise pulse voltage, peak noise pulse voltage and noise pulse width (see 3.3).

3.1 General considerations.

3.1.1 Package test configuration. It is important to ground the package using the same pins as would be used in the microcircuit application. If the package has an internal ground plane or ground section, this should be connected via package pins(s) to the exterior test set-up ground plane. The package should be connected to the test set-up with coaxial cable or stripline. Unshielded conductor medium should not be used between the signal source and package. Coaxial shields must be grounded at both ends of the cable. Package sockets should not be used unless these are to be part of the microcircuit application configuration. Package leads must be formed and trimmed as specified in the application. Package-to-chip interconnecting media shall be installed in the package and used to connect to the load resistors.

3.1.2 Pin selection. For simple packages with symmetrical, parallel pin conductors, only a sample of pin combinations need be tested. Unless otherwise specified by the procurement document, all combinations adjacent to the ground pin(s) and a combination opposite the ground pin(s) shall be tested, as a minimum. Complex packages with non-parallel conductors or multilayer wiring shall be tested for all adjacent-pair combinations unless otherwise specified.

3.2 Coupling capacitance measurements. Connect the test equipment as shown in figure 30XX.1-1. Use a 50-ohm chip resistor load in the driven pin channel unless otherwise specified. For the pick-up pin channel, use the load resistor value(s) as specified by the procurement document. (Load resistor values should be set such that the parallel combination of load resistance and probe impedance matches as closely as practical the specified load impedance of a single receiver in the logic system to be used in the microcircuit application.) Check the residual cross-coupling of the measuring set-up by touching the probe to the pick-up channel load before the pick-up pin is connected to the resistor. Measure and record the peak pulse voltage observed. This peak pulse reading must be less than 50% of the reading observed with the pin connected to the resistor for a reading to be valid. Adjust the test set-up cable orientation and configuration to minimize this residual cross-coupling.

Connect the pick-up pins to the load resistor and adjust the pulse width so that the time required to charge the coupling capacitance to 0V can be observed. Measure the time at the 63% voltage point on the waveform (T) and calculate coupling capacitance (C_C) as follows:

$$\text{Determine } R_{Total} = \frac{R_{Probe} \times R_{Load}}{R_{Probe} + R_{Load}}$$

$$C_{Total} = \frac{T}{R_{Total}}$$

$$C_C = C_{Total} - C_{Probe}$$

Values of C_C can be used as a relative measure for comparison of potential crosstalk among several packages to a standard package. The coupling capacitance (C_C) can also be used to predict levels of crosstalk for various logic systems or circuit configurations by performing a pulse response analysis using a circuit simulator.

3.3 Noise pulse Measurements. Using the same test setup as in 3.2, measure the crosstalk noise pulse voltage at the minimum noise pulse width specified for the logic system or as specified by the procuring agency.

Measure the peak noise voltage value of the coupled crosstalk.

4. SUMMARY. The following details, when applicable, shall be specified in the procurement document:

a. C_C
b. V_{OL} (max)
c. V_{OH} (min)
d. V_{IL} (max)
e. V_{IH} (min)
f. t_{PL}
g. t_{PH}
h. t_{tLH}
i. t_{tHL}
j. V_N
k. V_{NPK}

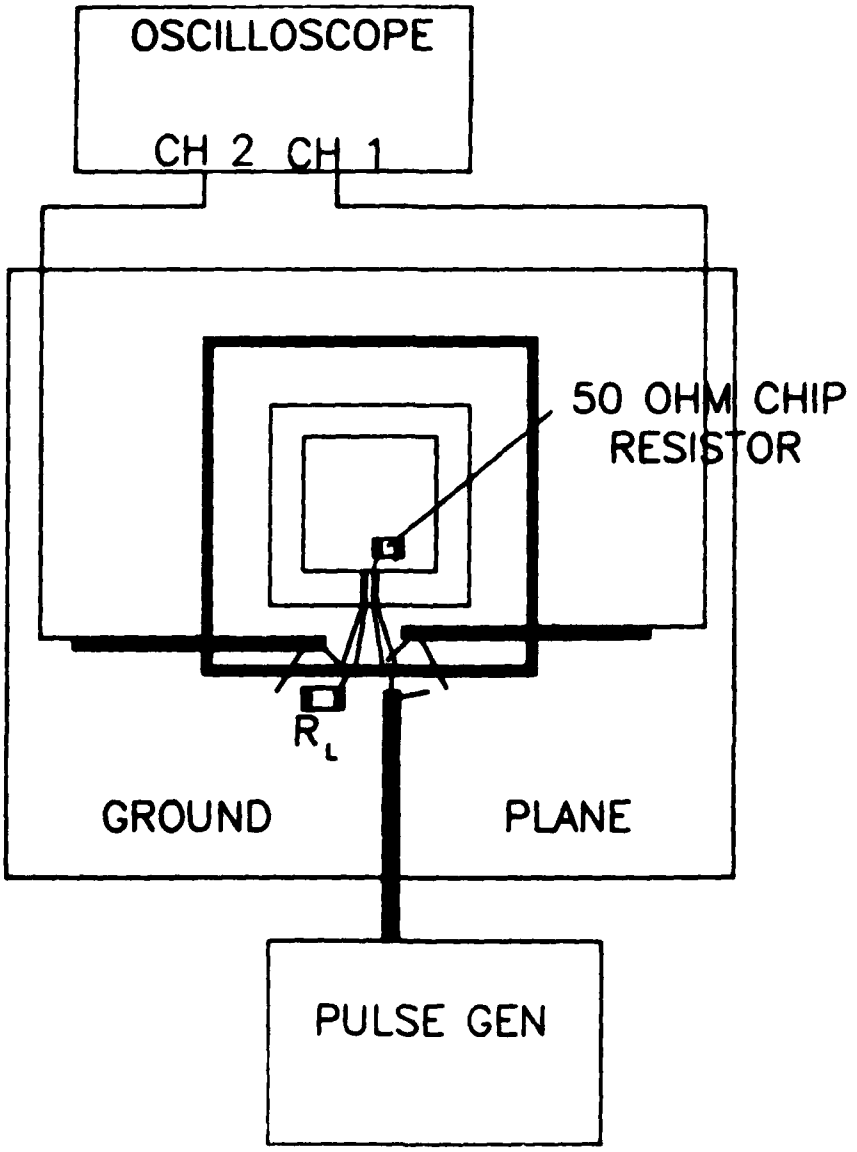


Figure 30XX.1-3 - Crosstalk Measurement Test Equipment Configuration.

METHOD 30XX.1

GROUND AND POWER SUPPLY IMPEDANCE MEASUREMENTS
FOR DIGITAL MICROELECTRONICS DEVICE PACKAGES

1. PURPOSE. This method establishes the means of measuring the series impedance of the ground and power supply circuit pin configurations for packages used for complex, wide bandwidth digital microcircuits. The method provides data that are useful in the evaluation of the relative performance of various packages and can be used to predict the contribution of the package to power supply noise and ground noise.

1.1 Definition.

1.1.1 Ground or power supply impedance. The series combination of inductive reactance and resistance exhibited by all of the conductor paths between the semiconductor chip interface and the exterior package--interface in either the ground circuit or the power supply circuit. The impedance of a series inductive circuit is defined by the equation

$$Z = \sqrt{R^2 + X^2_L} \quad .$$

1.2 Symbols. The following symbols shall apply for purposes of this test method and shall be used in conjunction with the definition provided in 1.1:

L_G: series inductance of the ground circuit path in a package (henries).

L_P: series inductance of the power supply circuit path in a package (henries).

X_G: series inductive reactance of ground path = $2\pi f L_G$ (ohms).

X_P: series inductive reactance of power supply path = $2\pi f L_P$ (ohms).

f: frequency (Hz).

f_{tr}: frequency of primary component of digital pulse transition = $\frac{1}{t_t}$ (Hz).

f_{tp}: frequency related to noise pulse width specified for the logic system: $f_{tp} = \frac{1}{tp_{min}}$ (Hz).

t_t: transition time from logic system. Equal to the smaller value of LOW to HIGH or HIGH to LOW transition.

Z_G: series impedance of ground path at frequency: $Z_G = \sqrt{R_G^2 + X_G^2}$.

Z_P: series impedance of power supply path at frequency: $Z_P = \sqrt{R_P^2 + X_P^2}$.

t_{Pmin}: The minimum noise pulse width at either the V_{IH} or V_{IL} level specified for a given logic system.

2. APPARATUS. The apparatus used for ground impedance measurements shall include a suitable RF inductance meter and a suitable milliohmmeter.

2.1 RF inductance meter. The RF inductance meter (or multi-frequency LCR meter) shall be capable of AC measurements of series inductance over the range of 1 nanohenry to 1000 nanohenries at a frequency of 100 KHz with an accuracy of $\pm$ 5% including test fixture errors.

2.2 Milliohmmeter. The milliohmmeter (or LCR meter) shall be capable of measuring resistance using a 4-wire method over the range from 10 milliohms to 10 ohms with an accuracy of $\pm$5%, including test fixture errors.

3. PROCEDURE. Measurement of series ground impedance (Z_G) and power supply impedance (Z_P) shall be made for all standard power and ground configurations specified for the package application. Measurements shall be performed in accordance with 3.2.

3.1 General considerations. Accurate measurement of series impedance requires careful design and implementation of test adapters to minimize errors. Since the inductance and resistance values being measured are usually quite small, means must be provided to null out the tare resistance and inductance of the test adapters through 4-wire methods and subtraction techniques. The tare values of the interconnecting circuits must be small to enable the meters to read on ranges that provide adequate resolution and accuracy. The techniques specified herein are adequate for predicting impedance at frequencies up to 1 GHz. Impedance shall be evaluated at a frequency related to either the transition time ($f_{tr} = \frac{1}{t_{tr}}$) or to the noise pulse width of the logic system used in the package ($f_{tp} = \frac{1}{t_{Pmin}}$). The frequency f shall be as specified in the procurement document.

The configuration of the package being tested must be the same as in the application. Wirebonds and other interconnection media must be included in the measurement. The package should be mounted on a dielectric holding fixture to avoid stray capacitance between the package and test equipment ground planes. Sockets should not be used unless specified. Package leads must be trimmed to applications specifications.

3.2 Test procedure for series impedance.

3.2.1 Series inductance. With the inductance meter, measure the series inductance of the power supply circuit (L_P) between the external package solder interface and the chip power supply location. Similarly, measure the inductance of the ground circuit (L_G). Calculate $X_P = 2\pi f L_P$ and $X_G = 2\pi f L_G$.

3.2.2 Series resistance. With the milliohmmeter, measure the series resistance of the same power and ground circuits: R_P and R_G.

3.2.3 Calculation of impedance.

$$\text{Calculate } Z_P = \sqrt{X_P^2 + R_P^2}$$

$$Z_G = \sqrt{X_G^2 + R_G^2}$$

4. SUMMARY. The following details, when applicable, shall be specified in the applicable procurement document.

a. Z_P (max)

b. Z_G (max)

c. L_P (max)

d. L_G (max)

e. R_P (max)

f. R_G (max)

g. f

h. f_{tr}

i. f_{tp}

j. t_t

k. t_{Pmin}

METHOD 20XX.1

FLIP-CHIP PULL-OFF TEST

1. PURPOSE. The purpose of this test is to measure the strength of internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bonds. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is greater.

3. PROCEDURE. The test shall be conducted using the procedure which follows. All die pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. The LTPD specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices, a minimum of 4 die or all die if four are not available on a minimum of 2 completed devices shall be used. All pull tests shall be performed prior to the application of encapsulants, adhesive, or any material which may increase the apparent bond strength.

When flip chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metalized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Testing. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or kovar wire) having a cross-sectional area of 75 percent, +3/-5 percent of the chip surface area. The rod shall make connection with a hard setting adhesive material (for instance, a cyanoacrylate or other adhesive possessing high tensile strength) on the back of the flip chip. The substrate

shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The die shall be pulled without shock, within 5 degrees of the normal at a rate of 500 grams + 100 grams per second, until the die separates from the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any flip-chip pull which results in separation under an applied stress less than 1780 kg/in^2 x average solder bump area (in^2) x number of solder bumps shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the predominant category of separation or failure shall be recorded:

a. Silicon broken.
b. Lifted metallization from chip.
c. Separation at bond-chip interface.
d. Failure within bond.
e. Separation at bond-substrate interface.
f. Lifted metallization from substrate.
g. Substrate broken.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

a. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.
b. LTPD, selection and number of die to be tested, if other than 4.
c. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).